Electronics Lab Manual

Howard T. Russell, Jr., PhD
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</table>
Lab Meeting No. 1

Introduction to EE Labs

I. Introduction
The objective of this first lab meeting is to reintroduce EE students to a professional laboratory environment where electronic circuits are built and electrical engineering experiments performed. The following topics will be addressed in this introductory meeting –

- an orientation regarding proper behavior and safety while in the lab,
- tools and tool box requirements,
- lab instruments,
- cables, connectors, probes, and wires,
- electronic components, parts, and the parts request form,
- lab report format,
- useful web sites, and
- lab rules.

II. Lab Orientation
All Electronics I & II students are required to attend an orientation regarding proper behavior and safety while in the lab. This orientation is presented by the resident lab technicians who are responsible for the maintenance and up-keep of the EE labs in Nedderman Hall.

III. Tools and Tool Box (Attachment A)
Basic items such as pliers, cutters, and wire strippers are integral components in any electrical engineer’s tool box. These tools are necessary to build circuits and perform experiments in the EE lab. Therefore, it is a mandatory requirement that all Electronics I & II students obtain and maintain a tool box containing a set of electrical engineering specific tools. The tool box requirement is not an option and all students must bring their tool box fully loaded to every lab meeting beginning with the second meeting. Students without a tool box on the second and subsequent lab meetings will not be allowed in the lab and will receive a zero for the lab. A list of these tools along with their photographs is included in Attachment A at the end of this document.

IV. Lab Instruments (Attachment B)
The electrical engineering labs located in rooms NH129, NH129A, NH148, and NH148A are equipped with the most current industry standard test and measurement equipment found in professional electrical engineering companies. Each lab is divided into a series of lab benches with each bench containing the following instruments –

- Agilent 34401A 6½ digit multimeter (DMM),
- Agilent E3620A dual dc power supply (25V, 1A),
- Agilent 54621A 60MHz dual channel oscilloscope, and
- Agilent 33120A 15MHz function generator.

Most of the experiments performed in the electronics labs will involve the above mentioned instruments to some degree. Data sheets for these instruments are included in Attachment B.

V. Cables, Connectors, Probes, and Wires
Each lab is equipped with one or more wall-mounted racks containing a variety of cables, connectors, oscilloscope probes, and wires. These connectors provide the necessary electrical connections among the bench instruments and your circuits.

VI. Electronic Components, Parts, and the Parts Request Form (Attachment C)
A wide assortment of electronic components and parts are available in the EE lab. An extensive list of components and parts can be found on the lab web site www-ee.uta.edu/eelabs2/. Click on ‘parts available’ for a view of the list. The experiments performed in the electronics labs involve the use of parts supplied by the lab GTA. In more advanced courses, students will have to order their own parts through the lab by submitting an online parts request form. A copy of this form is shown in Attachment C. Most of the parts listed on the lab web site are considered disposable. This means that once parts are given to the student, the student is allowed to keep and accumulate them. For parts not on the list, a formal written request for these parts may be submitted along with instructor approval to lab personnel.
VII. Lab Report Format (Attachment D)
Formal lab reports are due typically within one week after each lab experiment. Exceptions are made for more complex and/or extensive lab experiments. The format for lab reports is outlined below.
• Title Page. Every lab report begins with a title page. This page includes the course and section number, experiment number, experiment title, date the experiment was performed, date the report submitted, and student name and ID number. A sample of the lab report cover page is included in Attachment D.
• Introduction. A brief description of the purpose of the lab and a discussion of key information the reader will need to understand the experiment. Give a brief description of the theory the experiment is based upon.
• Procedure. Describe how the experiment was performed. List equipment, instruments, and components used in the experiment. Include the theory, equations, and detailed schematics of circuits involved.
• Results. Present the results of the experiment with data collected from measurements performed. Data should be professionally and neatly presented in the form of tables, graphs, and plots.
• Discussions. Discuss any new ideas and/or questions produced in the experimental process. Comment on the validity, accuracy, and usefulness of the procedure.
• Conclusion. A description of what the experiment revealed. Generate a comparison between the expected results based on theory and the actual results. An attempt should be made here to explain any discrepancies between these results.
• Appendix. The appendix should contain actual compiled data, notes and comments, equations, sketches, and schematics made during the experiment.
• References. List any material contributed from other sources.

VIII. Useful Web Sites
Mouser Electronics  www.mouser.com
Jameco Electronics  www.jameco.com
Electronics Express/RSR  www.elexp.com
Nuts and Volts (magazine)  www.nutsvolts.com

IX. Lab Rules
1. Regardless of the lab section, student attendance in all electronics labs is mandatory and not an option. You must attend each and every lab meeting for the entire time the lab is scheduled to be in session.
2. As indication of your attendance, you must sign and write the time of day on the lab attendance sheet provided at the beginning of each lab. If your signature and time stamp are not on the attendance sheet, you are considered to be absent and not in attendance for that lab meeting.
3. Do not sign for your lab partner(s) if they are not in attendance.
4. You must bring your tool box containing all required tools to each and every lab meeting. This is mandatory and not an option. The presence of your tool box will be checked off on the lab attendance sheet by the lab instructor or GTA. If you are in the lab without your tool box, you are considered to be absent and not in attendance for that lab meeting.
5. You are responsible for obtaining and applying data sheets for any and all components used in the lab experiments.
6. It is mandatory that the circuits you build and layout for the lab experiments work and perform as designed. This is not an option. You are responsible for trouble shooting your circuits and correcting any problems that cause them not to work.
7. Lab partners are well-advised to divide all tasks involved in lab experiments in an equal manner in order to gain experience in performing these tasks. For example, swap breadboard layout and measurement tasks so each partner becomes equally familiar with these jobs.
8. Formal lab reports are due on the date indicated. Reports submitted after the due date are considered late. Any late lab reports will not be counted in your lab grade.
9. A hands-on lab examination will be given at the end of the semester. This exam will be given to each student on a one-to-one basis with the instructor and/or GTA. The exam will test your ability and skills to
   • read a schematic diagram
   • build a circuit on a breadboard
   • measure voltage, current, and resistance
   • properly use and apply lab equipment.
10. Performance on the lab exam along with lab attendance and tool box is counted in the total lab grade.
11. If necessary, exceptions, additions, modifications, inclusions, and details to these and all other lab rules will be provided prior to or during the lab.
Attachment A

Tools and the Tool Box
August 2, 2009

<table>
<thead>
<tr>
<th>Component</th>
<th>Example Brand</th>
<th>Example Source</th>
<th>Price ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Suitable container (all-purpose plastic tool box; fishing tackle box)</td>
<td>Keter (13” all-purpose box)</td>
<td>Wal-Mart</td>
<td>3.64</td>
</tr>
<tr>
<td>Needle nose pliers (4” to 5”) (Figure 1)</td>
<td>Stanley (mini plier set)</td>
<td>Wal-Mart</td>
<td>12.88 (set of 6)</td>
</tr>
<tr>
<td>Diagonal cutters (4” to 5”) (Figure 2)</td>
<td>Stanley (mini plier set)</td>
<td>Wal-Mart</td>
<td></td>
</tr>
<tr>
<td>Wire strippers (5”) (Figure 3)</td>
<td>H-Tools (cutter and stripper, 34-899C)</td>
<td>Fry’s</td>
<td>3.49</td>
</tr>
<tr>
<td>Prototype breadboard (6.5” x 2” to 6.5” x 4” with 3 to 5 binding posts) (Figures 4 and 5)</td>
<td>Elenco (Model 9425, 6.5” x 2”, 830 test points)</td>
<td>Fry’s</td>
<td>9.99</td>
</tr>
<tr>
<td>Precision screwdriver set (6 to 11 piece set with slotted and Phillips screwdrivers) (Figure 6)</td>
<td>Stanley (6 piece; 4 slotted, 2 Phillips)</td>
<td>Wal-Mart</td>
<td>4.88</td>
</tr>
<tr>
<td>22 gauge solid hook-up wire (Figure 7)</td>
<td>Fry’s product number: PLU#1615281</td>
<td>Fry’s</td>
<td>2.99</td>
</tr>
</tbody>
</table>

*Tax: 3.09
Total: 40.96

Photos

**Figure 1**
5” needle-nose pliers
Figure 2
5” diagonal cutters

Figure 3
Wire strippers
Figure 4
Three binding post breadboard

Figure 5
Three binding post breadboard
Figure 6
Screwdriver set

Figure 7
22 gauge wire
Agilent 34401A Multimeter
Uncompromising Performance for Benchtop and System Testing

Product Overview

- Measure up to 1000 volts with 6½ digits resolution
- 0.0015% basic dcV accuracy (24 hour)
- 0.06% basic acV accuracy (1 year)
- 3 Hz to 300 kHz ac bandwidth
- 1000 readings/s direct to GPIB

Superior Performance
The Agilent Technologies 34401A multimeter gives you the performance you need for fast, accurate bench and system testing. The 34401A provides a combination of resolution, accuracy and speed that rivals DMMs costing many times more. 6½ digits of resolution, 0.0015% basic 24-hr dcV accuracy and 1,000 readings/s direct to GPIB assure you of results that are accurate, fast, and repeatable.

Use it on Your Benchtop
The 34401A was designed with your bench needs in mind. Functions commonly associated with bench operation, like continuity and diode test, are built in. A Null feature allows you to remove lead resistance and other fixed offsets in your measurements. Other capabilities like min/max/avg readouts and direct dB and dBm measurements make checkout with the 34401A faster and easier.

The 34401A gives you the ability to store up to 512 readings in internal memory. For trouble-shooting, a reading hold feature lets you concentrate on placing your test leads without having to constantly glance at the display.

Use it for Systems Testing
For systems use, the 34401A gives you faster bus throughput than any other DMM in its class. The 34401A can send up to 1,000 readings/s directly across GPIB in user-friendly ASCII format.

You also get both GPIB and RS-232 interfaces as standard features. Voltmeter Complete and Externat Trigger signals are provided so you can synchronize to other instruments in your test system. In addition, a TTL output indicates Pass/Fail results when limit testing is used.

To ensure both forward and backward compatibility, the 34401A includes three command languages (SCPI, Agilent 3478A and Fluke 8840A / 42A), so you don’t have to rewrite your existing test software. An optional rack mount kit is available.

Easy to Use
Commonly accessed attributes, such as functions, ranges, and resolution are selected with a single button press.

Advanced features are available using menu functions that let you optimize the 34401A for your applications.

The included Agilent IntuiLink software allows you to put your captured data to work easily, using PC applications such as Microsoft Excel or Word to analyze, interpret, display, print, and document the data you get from the 34401A. You can specify the meter setup and take a single reading or log data to the Excel spreadsheet in specified time intervals. Programmers can use ActiveX components to control the DMM using SCPI commands. To find out more about IntuiLink, visit www.agilent.com/find/intuiink

1-Year Warranty
With your 34401A, you get full documentation, a high-quality test lead set, calibration certificate with test data, and a 1-year warranty, all for one low price.

Agilent Technologies
### Accuracy Specifications ± (% of reading + % of range)\(^1\)

<table>
<thead>
<tr>
<th>Function</th>
<th>Range (^2)</th>
<th>Frequency, etc.</th>
<th>24 Hour (^3) 23°C ±1°C</th>
<th>99 Day 23°C ±5°C</th>
<th>1 Year 23°C ±5°C</th>
<th>Temperature Coefficient (^4) 6°C to 18°C 23°C to 50°C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC voltage</strong></td>
<td>100.000 mV</td>
<td>0.0400 ± 0.0000</td>
<td>0.0640 ± 0.0000</td>
<td>0.0600 ± 0.0000</td>
<td>0.0005 ± 0.0005</td>
<td>0.0005 ± 0.0005</td>
</tr>
<tr>
<td></td>
<td>1.00000 mV</td>
<td>0.0400 ± 0.0002</td>
<td>0.0640 ± 0.0005</td>
<td>0.0600 ± 0.0006</td>
<td>0.0005 ± 0.0001</td>
<td>0.0005 ± 0.0005</td>
</tr>
<tr>
<td></td>
<td>10.00000 mV</td>
<td>0.0400 ± 0.0008</td>
<td>0.0640 ± 0.0007</td>
<td>0.0600 ± 0.0008</td>
<td>0.0005 ± 0.0004</td>
<td>0.0005 ± 0.0004</td>
</tr>
<tr>
<td></td>
<td>100.00000 mV</td>
<td>0.0400 ± 0.0009</td>
<td>0.0640 ± 0.0009</td>
<td>0.0600 ± 0.0010</td>
<td>0.0005 ± 0.0005</td>
<td>0.0005 ± 0.0005</td>
</tr>
<tr>
<td><strong>AC voltage</strong></td>
<td>100.000 mV</td>
<td>0.0400 ± 0.0001</td>
<td>0.0640 ± 0.0002</td>
<td>0.0600 ± 0.0003</td>
<td>0.0005 ± 0.0001</td>
<td>0.0005 ± 0.0001</td>
</tr>
<tr>
<td></td>
<td>5 Hz – 10 Hz</td>
<td>0.0400 ± 0.0004</td>
<td>0.0640 ± 0.0006</td>
<td>0.0600 ± 0.0006</td>
<td>0.0005 ± 0.0001</td>
<td>0.0005 ± 0.0001</td>
</tr>
<tr>
<td></td>
<td>5 Hz – 10 Hz</td>
<td>0.0400 ± 0.0005</td>
<td>0.0640 ± 0.0007</td>
<td>0.0600 ± 0.0007</td>
<td>0.0005 ± 0.0002</td>
<td>0.0005 ± 0.0002</td>
</tr>
<tr>
<td></td>
<td>5 Hz – 10 Hz</td>
<td>0.0400 ± 0.0006</td>
<td>0.0640 ± 0.0008</td>
<td>0.0600 ± 0.0008</td>
<td>0.0005 ± 0.0003</td>
<td>0.0005 ± 0.0003</td>
</tr>
<tr>
<td></td>
<td>5 Hz – 10 Hz</td>
<td>0.0400 ± 0.0007</td>
<td>0.0640 ± 0.0009</td>
<td>0.0600 ± 0.0010</td>
<td>0.0005 ± 0.0004</td>
<td>0.0005 ± 0.0004</td>
</tr>
<tr>
<td></td>
<td>5 Hz – 10 Hz</td>
<td>0.0400 ± 0.0008</td>
<td>0.0640 ± 0.0010</td>
<td>0.0600 ± 0.0011</td>
<td>0.0005 ± 0.0005</td>
<td>0.0005 ± 0.0005</td>
</tr>
<tr>
<td><strong>Resistance</strong></td>
<td>1000.000 (\Omega)</td>
<td>1 mΩ Current Source</td>
<td>0.0000 ± 0.0001</td>
<td>0.0000 ± 0.0001</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0002</td>
</tr>
<tr>
<td></td>
<td>1 mΩ Current Source</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0004</td>
</tr>
<tr>
<td></td>
<td>100.000 (\Omega)</td>
<td>0.0000 ± 0.0001</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0003</td>
</tr>
<tr>
<td></td>
<td>10.000 (\Omega)</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0004</td>
</tr>
<tr>
<td></td>
<td>1.000 (\Omega)</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0005</td>
<td>0.0000 ± 0.0005</td>
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<tr>
<td></td>
<td>100.0 (\Omega)</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0005</td>
<td>0.0000 ± 0.0005</td>
<td>0.0000 ± 0.0006</td>
<td>0.0000 ± 0.0006</td>
</tr>
<tr>
<td></td>
<td>10.0 (\Omega)</td>
<td>0.0000 ± 0.0006</td>
<td>0.0000 ± 0.0007</td>
<td>0.0000 ± 0.0007</td>
<td>0.0000 ± 0.0008</td>
<td>0.0000 ± 0.0008</td>
</tr>
<tr>
<td><strong>DC current</strong></td>
<td>10.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0000</td>
<td>0.0000 ± 0.0000</td>
<td>0.0000 ± 0.0000</td>
<td>0.0000 ± 0.0000</td>
</tr>
<tr>
<td></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0001</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0002</td>
</tr>
<tr>
<td></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0002</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0004</td>
</tr>
<tr>
<td><strong>True rms</strong></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0003</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0005</td>
</tr>
<tr>
<td><strong>AC current</strong></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0004</td>
<td>0.0000 ± 0.0005</td>
<td>0.0000 ± 0.0005</td>
<td>0.0000 ± 0.0006</td>
</tr>
<tr>
<td></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0005</td>
<td>0.0000 ± 0.0006</td>
<td>0.0000 ± 0.0006</td>
<td>0.0000 ± 0.0007</td>
</tr>
<tr>
<td></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0006</td>
<td>0.0000 ± 0.0007</td>
<td>0.0000 ± 0.0007</td>
<td>0.0000 ± 0.0008</td>
</tr>
<tr>
<td></td>
<td>1.00000 mA</td>
<td>&lt; 0.1 V</td>
<td>0.0000 ± 0.0007</td>
<td>0.0000 ± 0.0008</td>
<td>0.0000 ± 0.0008</td>
<td>0.0000 ± 0.0009</td>
</tr>
</tbody>
</table>

1. Specifications are for 1 hour warm-up and 1-digit display slow ac filter.
2. Relative to calibration standards.
3. 25% lower range set range except: 1000 Vdc and 750 Vac ranges.
4. For low-range input: 5% of range. For inputs from 1% to 5% of range and < 50 kHz, add 0.1% of range additional error.
5. For 50 V range limited to 100 kHz or 10 Vdc, 3 kHz.
6. Typically 10% of reading error at 1 MHz.
7. Specifications are for 4-20mA function or 2wire ohms using Math Null. Without Math Null: add 4.2 mA additional error to 2wire ohms function.
8. Input > 100 mA. For 10 mA to 160 mA inputs multiply % of reading error x10
9. Accuracy specifications are for the voltage measured at the input terminals only. 1 mA test current is typical. Variation in the current source will cause some variation in the voltage drop across a diode junction.

---

[Diagram and notes]
Measurement Characteristics

DC Voltage

Measurement Method:
Continuously integrating multi-slope III
A-D converter.
A-D Linearity:
0.0002% of reading + 0.0001% of range
Input Resistance:
10 MΩ or 0.1 V / 1 V, 10 V ranges:
Selectable > 10,000 MΩ
100 V, 1000 V ranges: 10 MΩ ±1%
Input Bias Current:
< 30 pA at 25°C
Input Protection:
1000 V rms all ranges
dV/dt ratio accuracy:
V_input Accuracy + V_pulsed Accuracy

True RMS AC Voltage

Measurement Method:
AC-coupled true rms measures the ac component of the input with up to 100 Vdc of bias on any range.
 Crest Factor:
Maximum of 5:1 at full scale.
Additional Crest Factor errors (non-sinusoidal):
Crest factor 1-2: 0.05% of reading
Crest factor 2-3: 0.15% of reading
Crest factor 3-4: 0.30% of reading
Crest factor 4-5: 0.40% of reading
Input Impedance:
1 MΩ ± 2% in parallel with 100 pF
Input Protection: 750 V rms all ranges

Resistance

Measurement Method:
Selects one of 4 wires or 2-wire Ohms.
Current source referenced to LO input.
Maximum Lead Resistance (4-wire):
10% of range per wire for 100 Ω, 1 kΩ per wire for all other ranges.
Input Protection: 1000 V rms all ranges

DC Current

Short Resistance:
5.2 Ω for 10 mA, 100 mA
0.1 Ω for 1 A, 3 A
Input Protection:
Externally accessible 3 A 250 V fuse
Internal 7 A 250 V fuse

True RMS AC Current

Measurement Method:
Directly coupled to the fuse and shunt
ac-coupled true rms measurement (measures the ac component only).
Shunt Resistance:
0.1 Ω for 1 A, 3 A ranges
Input Protection:
Externally accessible 3 A 250 V fuse
Internal 7 A 250 V fuse

Frequency and Period

Measurement Method:
Reciprocal counting technique
Voltage Ranges:
Same ac voltage function
Gain Time: 1 s, 100 ms, or 10 ms
Continuity/Diode
Response Time:
300 samples/s with audible tone
Continuity Threshold:
Selectable from 1 Ω to 1000 Ω

Measurement Noise Rejection 60 (50) Hz¹

dc CMRR: 110 dB
ac CMRR: 71 dB

Integration Time and Normal Mode Rejection:
10 pC/1.46 s (2 s): 50 dB³
10 pC/100 ns (200 ns): 60 dB³
1 pC/16.7 ms (20 ms): 60 dB
<1 pC/3 ms or 800 μs: 60 dB

Operating Characteristics¹

<table>
<thead>
<tr>
<th>Function</th>
<th>Digits</th>
<th>Reading/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>dV, dI, and</td>
<td>6½</td>
<td>0.6 (0.5)</td>
</tr>
<tr>
<td>Resistance</td>
<td>6½</td>
<td>0 (%)</td>
</tr>
<tr>
<td>5½</td>
<td>90-99%</td>
<td></td>
</tr>
<tr>
<td>4½</td>
<td>301</td>
<td></td>
</tr>
<tr>
<td>3½</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>mV, nC</td>
<td>6½</td>
<td>0.11 slow (1 Hz)</td>
</tr>
<tr>
<td>6½</td>
<td>1 nC (200 Hz)</td>
<td></td>
</tr>
<tr>
<td>6½</td>
<td>10 fast (200 Hz)</td>
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<tr>
<td>4½</td>
<td>50</td>
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Frequency

<table>
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<tr>
<th>Function</th>
<th>5½</th>
<th>9.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>4½</td>
<td></td>
<td>00</td>
</tr>
</tbody>
</table>

Frequency and Period

Configuration rates: 20/s to 20/s
Averaging rate (mv Volts): > 39/s
ASII readings to RS-232: 55/s
ASII readings to RS-232: 100/s
Maximum internal trig rate: 1000/s
Max. external rate to memory: 1000/s

Triggering and Memory

Reading HOLD Sensitivity:
10%, 1%, 0.1%, or 0.01% of range
Sample/Trigger:
1 to 10,000
Trigger Delay: 0 to 3000 ± 10 ms step size
External Trigger Delay: < 1 ms
External Trigger Jitter: < 500 μs
Memory: 512 readings

Math Functions

null min/max/average, d6m, dB, limit test
(with TTL output)

Standard Programming Languages

SCPI (IEEE 488.2), Agilent 34760A,
Riken 9944A/42A

Accessories Included

Test lead kit with probe, alligator
and grabber attachments
Operating manual, service manual,
test report and power cord

General Specifications

Power Supply:
100 V-120 V/220 V/240 V ±10%
Power Line Frequency:
45 Hz to 60 Hz and 50 Hz to 440 Hz
Automatically sensed 50 Hz/60 Hz
Power Consumption:
15 W peak (10W average)
Operating Environment:
Full accuracy for 0°C to 55°C,
Full accuracy to 80% RH. at 40°C
Storage Temperature: -40°C to 70°C
Weight: 3.6 kg (8 lbs)
Safety: Designed to Csa, UL-1244, IEC-348
RR and ESD:
MIL-461C, FTZ, 104E, FOC
Vibration & Shock:
MIL-T-28800F, Type III, Class 5 (air only)
Warranty: 1 year

¹ For 1 Ω unbalanced in LO bias, ±500 V peak maximum.
² For power line frequency ± 11 kHz.
³ For power line frequency ± 11% ± 4 dB.
⁴ Reading speed of 60 Hz and analog operation.
⁵ Maximum 40% of drift (settable settling times).
⁶ Spacing arc for 4½ digits, date, time, and display.
Ordering Information

Agilent 34401A multimeter accessories included:
- Test lead kit with probe, alligator, and grabber attachments, operating manual, service manual, calibration certificate, test report, and power cord.

Options
- 34401A-1CM
  Back mount kit*  
  (P/N 56003-0240)
- 34401A-080
  DMM without manuals
- 34401A-AJ
  ANSI Z240 compliant calibration

Manual Options
(Please specify one)
- 34401A-ABA US English
- 34401A-ABD German
- 34401A-ABE Spanish
- 34401A-ABF French
- 34401A-ABJ Japanese
- 34401A-ABZ Italian
- 34401A-AB0 Taiwanese Chinese
- 34401A-AB1 Korean
- 34401A-AB2 Chinese
- 34401A-AKX Russian

Agilent Accessories
- 11069A Kelvin probe set
- 11080A Surface mount device (SMD) test probes
- 11082A Kelvin clip set
- 3413I Hard transit case
- 34101A Accessory pouch
- 34171B Input terminal connector (sold in pairs)
- 34172B Input calibration short (sold in pairs)
- 34330A 30 A current shunt
- E2398A 5 k thermistor probe

* Forracking two side-by-side, order both items below:
  - Lock link kit (P/N 5601-0694)
  - Flange kit (P/N 5603-6212)

Remove all doubt

Our repair and calibration services will get your equipment back to you, performing like new, when promised. You will get full value out of your Agilent equipment throughout its lifetime. Your equipment will be serviced by Agilent-trained technicians using the latest factory calibration procedure, automated repair diagnostics and genuine parts. You will always have the utmost confidence in your measurements.

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www.lixstandard.org
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www.agilent.com
For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:
www.agilent.com/find/contactus

Americas

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<thead>
<tr>
<th>Country</th>
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<tbody>
<tr>
<td>Canada</td>
<td>(877) 694-4414</td>
</tr>
<tr>
<td>Latin America</td>
<td>305 269 7590</td>
</tr>
<tr>
<td>United States</td>
<td>(800) 829-4444</td>
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Asia Pacific

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<tr>
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<tbody>
<tr>
<td>Australia</td>
<td>1 800 629 469</td>
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<tr>
<td>China</td>
<td>800 810 0189</td>
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<tr>
<td>Hong Kong</td>
<td>800 938 692</td>
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<td>India</td>
<td>1 800 112 929</td>
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<td>Japan</td>
<td>0120 (421) 345</td>
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<tr>
<td>Korea</td>
<td>050 769 0000</td>
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<td>Malaysia</td>
<td>1 800 868 810</td>
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<td>Singapore</td>
<td>1 800 375 8100</td>
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<tr>
<td>Taiwan</td>
<td>0900 947 906</td>
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<td>Thailand</td>
<td>1 800 215 068</td>
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Europe & Middle East

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<tr>
<td>Austria</td>
<td>0220 07 44 11</td>
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<tr>
<td>Belgium</td>
<td>32 (0) 2 404 93 44</td>
</tr>
<tr>
<td>Denmark</td>
<td>45 70 13 1515</td>
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<tr>
<td>Finland</td>
<td>358 (0) 10 855 2190</td>
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<tr>
<td>France</td>
<td>0225 010 700*</td>
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<tr>
<td>Germany</td>
<td>01605 24 6333**</td>
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<tr>
<td>Ireland</td>
<td>1990 024 260</td>
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<tr>
<td>Israel</td>
<td>972-3-3288-504/544</td>
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<tr>
<td>Italy</td>
<td>39 02 92 60 648</td>
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<tr>
<td>Netherlands</td>
<td>31 (0) 20 547 2111</td>
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<tr>
<td>Spain</td>
<td>34 (91) 631 3300</td>
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<tr>
<td>Sweden</td>
<td>0200 06 22 95</td>
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<tr>
<td>Switzerland (French)</td>
<td>41 (21) 81 1381 (Opt 2)</td>
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<tr>
<td>Switzerland (German)</td>
<td>0800 00 53 33 (Opt 1)</td>
</tr>
<tr>
<td>United Kingdom</td>
<td>41 (0) 116 0276201</td>
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</tbody>
</table>

Other European Countries:
www.agilent.com/find/contactus

Revised October 24, 2007

Product specifications and descriptions in this document subject to change without notice.

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5068-0112EN
Agilent
E36XXA Series
Non-Programmable DC Power Supplies

Data Sheet
Reliable Power, Repeatable Results

- Linear power supply
- Single, dual or triple output
- 10-turn voltage and current control
- Low noise and excellent regulation

Affordable, full-featured benchtop power supplies provide excellent performance and flexibility

A whole family of low-cost power supplies to meet your needs

The E3600 Series of low-cost benchtop power supplies give you the performance of high-end supplies at a decent price. All E3600 family members provide clean power with excellent regulation and a fast transient response. The E3640 Series single-output non-programmable models are described on this page. Refer to page 3 for information on dual-output and triple-output non-programmable models.

Single-output models

All E3600 Series single-output non-programmable power supplies feature separate digital panel meters for monitoring voltage and current simultaneously. All models also feature 10-turn potentiometers for accurate adjustment of voltage and current output settings.

With 0.01 percent load and line regulation, these instruments keep the output steady when power line and load changes occur.

The low normal mode noise specification of less than 200 μVrms ensures clean power for precision circuitry.

In all single-output models, either the positive or negative terminal can be connected to ground, providing a positive or negative voltage output. Outputs also can be floated up to 240 V from ground.

These instruments also feature adjustable current limits, letting you set the safest current limit without having to short the output.

E3610A, E3611A, and E3612A single-output, dual range models

These popular 30-watt bench supplies are designed for general laboratory use. The constant-voltage, constant-current output allows operation as either a voltage or current source. The changeover occurs automatically, based on the load. Each of these models has two ranges, allowing more current at a lower voltage. For higher output voltages, supplies can be connected in series. These models also feature overload protection. A continuously acting constant current circuit protects the power supply against all overloads including a direct short placed across the terminals in a constant voltage operation.

E3614A, E3615A, E3616A and E3617A models feature overvoltage protection, remote sensing and remote programming

These flexible 30-watt, single-range supplies can be used as either voltage or current source. When the output terminal voltage increases to a preset shut-down level, an overvoltage protection circuit disables the output to protect the device under test (DUT) for damage. The overvoltage protection feature can be easily monitored and adjusted from the front panel.

Using the remote sensing capability, these instruments automatically compensate for voltage drop in the load leads, so you obtain an accurate voltage at the DUT.

Using the remote analog voltage programming capability, these instruments can remotely vary the voltage, so you are able to control the regulation output voltage or current.

You can combine multiple units in auto-parallel, auto-series and auto-tracking configurations for greater output voltage or current capacity. Front and rear output terminals allow for a flexible configuration. The output voltage and current can be controlled with external 0 to 10 volt analog voltage or variable resistance.
Multiple-output non-programmable models

With multiple supplies in a compact unit, the E3610A and E3610B provide excellent performance while saving space on your bench. Both instruments feature a tight 0.01 percent line and load regulation and a low normal mode noise specification of less than 0.35 mV to ensure clean power for precision circuitry. With a common mode current specification of less than 1 µA, both multiple-output power supplies minimize the power line current injection.

Like the single-output models in the E3614 Series, the E3620A and E3630A feature separate digital panel meters so you can monitor the voltage and current simultaneously. They also protect your DUT against overload and short-circuit damage.

Smooth turn-on and turn-off transitions keep power spikes out of your circuits. Auto-tracking permits equal or proportional voltage sharing, and allows control of output voltage from one master unit. The master and slave supplies have the same output polarity with respect to a common bus or ground. This operation is useful where simultaneous turn-up, turn-down or proportional control of all power supplies is required.

E3620A dual-output power supply

The 50-watt E3620A dual-output power supply provides two 0 V to 25 Vdc outputs with the maximum current of 1 A to satisfy most bench requirements. The outputs are completely independent and isolated.

E3630A triple-output power supply with auto-tracking feature

The 35-watt E3630A triple-output power supply provides three DC outputs: 0 to 6 V with a maximum current of 1 to 2.5 A and 0 to 20 V and 0 to −20 V with a maximum current of 0.5 A. An auto-tracking feature lets you set one voltage control to adjust the +20 V and −20 V outputs simultaneously. The outputs track each other to within 1 percent, making it easy to adjust the power supply for circuits requiring balanced voltages.

Specifications

<table>
<thead>
<tr>
<th>Features</th>
<th>E3610A</th>
<th>E3611A</th>
<th>E3612A</th>
<th>E3614A</th>
<th>E3615A</th>
<th>E3616A</th>
<th>E3617A</th>
<th>E3620A</th>
<th>E3630A</th>
<th>E3638A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual range, 10 turn pots, Constant Voltage (CV), Constant Current (CC) modes.</td>
<td></td>
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<tr>
<td>Adjustable overvoltage protection, voltage &amp; resistance programming, remote sense, rear outputs, ten turn pots, CC, CC modes. Multiple supplies can be connected for tracking or higher power.</td>
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<tr>
<td>Isolated dual outputs, 10 turn pots CC, CL</td>
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<tr>
<td>Tracking CV, CL (±20 V) CV, CF (±6 V)</td>
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<tr>
<td>Number of outputs</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Number of Output Ranges</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DC Output Rating</td>
<td>8 V, 3 A</td>
<td>20 V, 1.5 A</td>
<td>60 V, 0.5 A</td>
<td>9 V, 6 A</td>
<td>20 V, 3 A</td>
<td>35 V, 1.7 A</td>
<td>60 V, 1 A</td>
<td>25 V, 1 A</td>
<td>25 V, 1 A</td>
<td></td>
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<tr>
<td>Load and Line Regulation</td>
<td>&lt; 0.01% + 2 mV</td>
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<tr>
<td>Supply and Noise (20 Hz to 20 kHz)</td>
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<tr>
<td>Normal mode voltage</td>
<td>&lt; 200 pVrms, &lt; 2 mVpp</td>
<td>&lt; 200 pVrms, &lt; 1 mVpp</td>
<td>&lt; 200 pVrms, &lt; 2 mVpp</td>
<td>&lt; 200 pVrms, &lt; 2 mVpp</td>
<td>&lt; 200 pVrms, &lt; 2 mVpp</td>
<td>&lt; 200 pVrms, &lt; 2 mVpp</td>
<td>&lt; 350 pVrms, &lt; 1.5 mVpp</td>
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<td></td>
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<tr>
<td>Normal mode current</td>
<td>&lt; 0.02% + 3 mA</td>
<td>&lt; 0.02% + 1.5 mA</td>
<td>&lt; 0.02% + 1 mA</td>
<td>&lt; 0.02% + 1 mA</td>
<td>&lt; 0.02% + 1 mA</td>
<td>&lt; 0.02% + 1 mA</td>
<td>&lt; 0.02% + 1 mA</td>
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<tr>
<td>Common mode current</td>
<td>Not specified</td>
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<tr>
<td>Common mode current</td>
<td>&lt; 1 µAms</td>
<td></td>
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<td></td>
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<tr>
<td>Transient Response Time</td>
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<tr>
<td>&lt; 50 µsec following a change in output current from full load to half load for output to recover within:</td>
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<tr>
<td>10 mV</td>
<td>15 mV</td>
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<tr>
<td>Meter Accuracy</td>
<td>±0.5% + 2 counts at 25 °C ± 5 °C</td>
<td></td>
<td></td>
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<td>Meter Resolution</td>
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<tr>
<td>Voltage</td>
<td>10 mV</td>
<td>100 mV</td>
<td>100 mV</td>
<td>10 mV</td>
<td>10 mV (0−20 V), 100 mV (±20 V)</td>
<td>10 mV</td>
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<tr>
<td>Current</td>
<td>10 mA</td>
<td>10 mA</td>
<td>1 mA</td>
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<td>1 mA</td>
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<td>Isolation</td>
<td>240 Vdc</td>
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### Supplemental Characteristics

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<th>E3611A</th>
<th>E3612A</th>
<th>E3614A</th>
<th>E3615A</th>
<th>E3616A</th>
<th>E3617A</th>
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<td>CV/CC</td>
<td>CV/CC</td>
<td>CV/CC</td>
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<tr>
<td>Temperature Coefficient per °C</td>
<td>&lt; 0.02% + 1 mV</td>
<td>&lt; 0.02% + 500 µV</td>
<td>&lt; 0.02% + 1 mV</td>
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<tr>
<td>Voltage</td>
<td>Current</td>
<td>&lt; 0.02% + 2 mA</td>
<td>&lt; 0.02% + 1 mA</td>
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<td></td>
<td>Voltage</td>
<td>&lt; 0.02% + 1 mA</td>
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<tr>
<td>Output Drift</td>
<td>Total drift for 3 hours</td>
<td>Less than 0.1% + 5 mV</td>
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<td></td>
<td>Total drift for 8 hours</td>
<td>N/A</td>
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<tr>
<td>Temperature Range</td>
<td>0 to 40°C for full rated output</td>
<td>0 to 40°C to 55°C</td>
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<td>Cooling</td>
<td>Convection cooling</td>
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<td>Isolation</td>
<td>±50 Vdc</td>
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<tr>
<td>AC Input</td>
<td>100 Vac ±10%, 47–63 Hz (op. 08)</td>
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<td></td>
<td>115 Vac ±10%, 47–63 Hz (op. 08)</td>
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<td></td>
<td>230 Vac ±10%, 47–63 Hz (op. 08)</td>
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<td>Weight</td>
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<td></td>
<td>5.6 kg (12.3 lbs) net, 6.75 kg (14.9 lbs) shipping</td>
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<td></td>
<td>6.0 kg (13.2 lbs) net, 6.35 kg (14.0 lbs) shipping</td>
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<tr>
<td></td>
<td>3.0 kg (6.6 lbs) net, 5.1 kg (11.3 lbs) shipping</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Size</td>
<td>20.1 mm H x 212.3 mm W x 318.4 mm D</td>
<td></td>
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<tr>
<td></td>
<td>3.5&quot; H x 8.4&quot; W x 12.5&quot; D</td>
<td></td>
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<tr>
<td></td>
<td>20.1 mm H x 212.3 mm W x 371.4 mm D</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>3.5&quot; H x 8.4&quot; W x 14.7&quot; D</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>20.1 mm H x 212.3 mm W x 392.4 mm D</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.5&quot; H x 8.4&quot; W x 15.4&quot; D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Warranty</td>
<td>One year for E3600 series power supplies</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Three months for standard shipped accessories</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Ordering Information

- **E3600 Series Power Supplies**
  - E3610A 30-Watt Power Supply
  - E3611A 30-Watt Power Supply
  - E3612A 30-Watt Power Supply
  - E3614A 30-Watt Power Supply
  - E3615A 30-Watt Power Supply
  - E3616A 30-Watt Power Supply
  - E3617A 30-Watt Power Supply
  - E3620A Dual-output Power Supply
  - E3630A Triple-output Power Supply

### Other Options

- Opt. L2 Extra manual
- Opt. UK8 Commercial calibration with test result data
- E3601A-108 Test load kit

### Standard Shipped Accessories

- User's guide, Product Reference CD, power cord

### Power Options

- Opt. 063 230 Vac ± 10%
- Opt. 06M 115 Vac ± 10%
- Opt. 06S 100 Vac ± 10%

### Rackmount Kits*

- E3614A/15A/16A/17A/20A
  - To rackmount two instruments side-by-side
  - Lock-link Kit (P/N 5061-984)
  - Range Kit (P/N 5063-9212)

### Extra Manual Sets

- E3611A/11A/12A Manual (P/N 5955-5304)
- E3614A/15A/16A/17A Manual (P/N 5955-5311)
- E3620A Manual (P/N 5962-9001)
- E3630A Manual (P/N 5955-5329)

### For a single instrument, also order

- Scanner panel (P/N 5402-3906)

* Rackmounting with ICM or lock-link/range kit requires:
  - Agilent or customer support rails
  - Agilent Support Rails-E3663AC.
Remove all doubt

Our repair and calibration services will get your equipment back to you, performing like new, when promised. You will get full value out of your Agilent equipment throughout its lifetime. Your equipment will be serviced by Agilent-trained technicians using the latest factory calibration procedures, automated repair diagnostics and genuine parts. You will always have the utmost confidence in your measurements.

Agilent offers a wide range of additional expert test and measurement services for your equipment, including initial start-up assistance, onsite education and training, as well as design, system integration, and project management.

For more information on repair and calibration services, go to www.agilent.com/find/removealldoubt

Product specifications and descriptions in this document subject to change without notice.

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United States (800) 819-4444

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China 000 016 0189
Hong Kong 880 938 003
India 1 800 112 929
Japan 0120 0421 345
Korea 080 705 0800
Malaysia 1 800 888 848
Singapore 1 800 375 8100
Taiwan 0800 047 866
Thailand 1 800 226 000

Europe & Middle East

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Belgium 32 (0) 2 494 93 46
Denmark 45 70 13 15 15
Finland 358 (0) 406 55 2100
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Germany 070 344 6333
Ireland 1800 924 264
Israel 972 3 0390 584/544
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Agilent Technologies
Agilent Technologies
54600-Series Oscilloscopes
Data Sheet

Easily see what's happening in your mixed analog and digital designs

- 60 to 500 MHz, up to 2 GSa/s
- Unique 2 + 16-channel MSO and 2- or 4-channel models
- 4 MB to 8 MB MegaZoom deep memory standard
- Patented high-definition display system
- Flexible triggering including CAN, I2C, LIN, SPI, and USB
- Deep memory transfer over the interface bus

Multiple configurations to meet your needs

If you work with both analog and digital components, Agilent Technologies 54600-Series oscilloscopes can help you easily see more of what's going on in your designs. The unique 2 + 16-channel mixed signal oscilloscope (MSO) models and the traditional 2- and 4-channel models are optimized with just the capabilities you need for verifying and debugging designs that include A/Ds, D/A, DSPs, and embedded 8- or 16-bit microcontrollers. These scopes give you the tools you need to solve your mixed analog and digital engineering challenges more easily.

Ideal for mixed analog and digital analysis

Ideal for analyzing designs with both analog and digital components, the 54600-Series scopes combine three critical features:

- Up to 8 MB of MegaZoom deep memory comes standard so you can capture long, non-repeating signals, maintain high sample rates, and quickly zoom in on areas of interest
- A revolutionary ultra-responsive, high-definition display that lets you see more signal detail than ever before
- Flexible triggering that lets you easily isolate and analyze the complex signals and fault conditions common in mixed analog and digital designs. I2C, CAN, LIN, USB, and SPI triggering come standard. N2758A CAN trigger module option is also available.

This combination of capabilities is tailored to give you the measurement power you need to get your mixed analog and digital job done faster.

At Agilent Technologies, we focus on developing products that help you do your job better. That's why 54600-Series scopes are optimized for your needs. Choose the one that's right for your application and your budget.
Selection Guide

Figure 1. 2 + 16-channel mixed signal oscilloscope (MSO) family shown with 2- and 4-channel models.

<table>
<thead>
<tr>
<th>Model</th>
<th>Bandwidth</th>
<th>Maximum Sample Rate</th>
<th>Maximum Memory*</th>
<th>Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>54621A</td>
<td>60 MHz</td>
<td>200 MSa/s</td>
<td>4 MB</td>
<td>2</td>
</tr>
<tr>
<td>546210</td>
<td>60 MHz</td>
<td>200 MSa/s</td>
<td>4 MB</td>
<td>2+16</td>
</tr>
<tr>
<td>54622A</td>
<td>100 MHz</td>
<td>200 MSa/s</td>
<td>4 MB</td>
<td>2</td>
</tr>
<tr>
<td>54622B</td>
<td>100 MHz</td>
<td>200 MSa/s</td>
<td>4 MB</td>
<td>2+16</td>
</tr>
<tr>
<td>54624A</td>
<td>100 MHz</td>
<td>200 MSa/s</td>
<td>4 MB</td>
<td>4</td>
</tr>
<tr>
<td>54641A</td>
<td>350 MHz</td>
<td>2 GSa/s&quot;</td>
<td>8 MB</td>
<td>2</td>
</tr>
<tr>
<td>546410</td>
<td>350 MHz</td>
<td>2 GSa/s&quot;</td>
<td>8 MB</td>
<td>2+16</td>
</tr>
<tr>
<td>54642A</td>
<td>500 MHz</td>
<td>2 GSa/s&quot;</td>
<td>8 MB</td>
<td>2</td>
</tr>
<tr>
<td>546420</td>
<td>500 MHz</td>
<td>2 GSa/s&quot;</td>
<td>8 MB</td>
<td>2+16</td>
</tr>
</tbody>
</table>

* Maximum sample rate and memory are interlaced; deep memory is standard; no options needed.
Selection Guide (continued)

Figure 2. 2 + 16-channel mixed signal oscilloscope (MSO) allows you to view analog and digital content on one instrument.

Mixed-signal scopes
(models 54621D, 54622D, 54641D, and 54642D)

The mixed-signal oscilloscopes (MSO), with 2 analog channels and 16 digital channels, uniquely combine the detailed signal analysis of a scope with the multi-channel timing measurements of a logic analyzer. They let you see the complex interactions among your signals on up to 18 channels at the same time. No more guesswork and no more piecing around to see a few channels at a time. These scopes can easily conquer mixed analog and digital debugging problems that a traditional scope can’t begin to address, because they let you simultaneously test and monitor the high-speed digital control signals and the slower analog signals in your design.

4-channel scope
(model 54624A)

If your designs include heavy analog content, the 100-MHz 54624A will give you the channel count and measurement power you need, including MegaZoom deep memory, high-definition display, and flexible triggering. Whether you’re testing designs with four inputs, such as anti-lock brakes, or monitoring multiple outputs of a power supply, the 4-channel model helps you get your debug and verification done with ease.

2-channel scopes
(models 54621A, 54622A, 54641A, and 54642A)

The 2-channel models bring all the benefits of MegaZoom deep memory, high-definition display, and flexible triggering to those value-minded designers with lower channel requirements. They give you an affordable way to see long time periods while maintaining high sample rate so you can see details in your designs.
MegaZoom deep memory helps you determine how your signals are impacting each other. With shallow memory scopes, you have to choose whether you look at a slow analog signal or fast digital content. With up to 8 MB deep memory, you don’t have to choose — capture all of your data at once.

Revolutionary high-definition display reveals subtle details that most scopes won’t show you.

Standard RS-232 and parallel ports provide PC and printer connectivity.

Free IntuiLink PC software makes transfer of waveform data to PC fast and easy.

Intensity knob allows you to adjust the contrast on screen.

Built-in floppy drive makes it easy to save your work and update your system software.
Quick pan and zoom for analysis with MegaZoom’s instant response and optimum resolution.

Auto-scale lets you quickly display any active signals, automatically setting the vertical, horizontal and trigger controls for the best display, while optimizing memory.

QuickMeas gives you any three automated measurements with the push of a button. QuickPrint automatically prints your screen or saves to disk with automated file names.

Standard Serial Triggering includes CAN, PCI, LIN, SPI, and USB.

Built-in help is available in 11 languages. Simply press and hold the front-panel key of interest for a few seconds, and a help screen pops up to explain its function.

Maximum sample rate and resolution on every measurement. The scope automatically adjusts memory depth as you use it, so you get maximum sample rate and resolution on every measurement. You don’t even have to think about it.

2 analog and 16 digital channel MSOs allow you to see up to 18 time-aligned signals on your scope screen. Also available in 2- and 4-channel models.
# Performance Characteristics

**Acquisition: Analog Channels**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Sample Rate</td>
<td>54621A/D, 54622A/D, 54641A/D, 54642A/D: 200 MSa/s</td>
</tr>
<tr>
<td></td>
<td>54641A/D, 54642A/D: 2 GSa/sec interleaved 1 GSa/sec each channel</td>
</tr>
<tr>
<td>Max Memory Depth</td>
<td>54621A/D, 54622A/D, 54641A/D, 54642A/D: 4 MB interleaved, 2 MB each channel</td>
</tr>
<tr>
<td></td>
<td>54641A/D, 54642A/D: 8 MB interleaved, 4 MB each channel</td>
</tr>
<tr>
<td>Vertical Resolution</td>
<td>8 bits</td>
</tr>
<tr>
<td>Peak Detection</td>
<td>54621A/D, 54622A/D, 54641A/D, 54642A/D: 5 ns</td>
</tr>
<tr>
<td></td>
<td>54641A/D, 54642A/D: 1 ns @ max sample rate</td>
</tr>
<tr>
<td>Averaging</td>
<td>Selectable from 2, 4, 8, 16, 32, 64 ... to 16383</td>
</tr>
<tr>
<td>High Resolution Mode</td>
<td>54621A/D, 54622A/D, 54641A/D, 54642A/D: 12 bits of resolution when ≥500 ps/div, (average mode with s/ae = 1)</td>
</tr>
<tr>
<td></td>
<td>54641A/D, 54642A/D: 12 bits of resolution when ≥100 ps/div, (average mode with s/ae = 1)</td>
</tr>
<tr>
<td>Filter</td>
<td>Sinc/x interpolation (single shot BW = sample rate/4 or bandwidth of scope, whichever is less) with vectors on</td>
</tr>
</tbody>
</table>

**Acquisition: Digital Channels (54621D, 54622D, 54641D, and 54642D only)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Sample Rate</td>
<td>54621D, 54622D: 400 MSa/s interleaved, 200 MSa/s each channel</td>
</tr>
<tr>
<td></td>
<td>54641D, 54642D: 1 GSa/s</td>
</tr>
<tr>
<td>Max Memory Depth</td>
<td>54621D, 54622D: 8 MB interleaved, 4 MB ea. channel</td>
</tr>
<tr>
<td>Vertical Resolution</td>
<td>1 bit</td>
</tr>
<tr>
<td>Glitch Detection</td>
<td>5 ns</td>
</tr>
<tr>
<td>(minimum pulse width)</td>
<td></td>
</tr>
</tbody>
</table>

**Vertical System: Analog Channels**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Channels</td>
<td>54621A/D, 54622A/D, 54641A/D, 54642A/D: Ch 1 and 2 simultaneous acquisition</td>
</tr>
<tr>
<td></td>
<td>54642A/D: Ch 1, 2, 3 and 4 simultaneous acquisition</td>
</tr>
<tr>
<td>Bandwidth (-3dB)*</td>
<td>54621A/D: dc to 98 MHz</td>
</tr>
<tr>
<td></td>
<td>54622A/D, 54640A: dc to 100 MHz</td>
</tr>
<tr>
<td></td>
<td>54641A/D: dc to 95 MHz</td>
</tr>
<tr>
<td></td>
<td>54642A/D: dc to 90 MHz</td>
</tr>
<tr>
<td>ac Coupled</td>
<td>54621A/D: 3.5 Hz to 60 MHz</td>
</tr>
<tr>
<td></td>
<td>54622A/D, 54640A: 3.5 Hz to 100 MHz</td>
</tr>
<tr>
<td></td>
<td>54641A/D: 3.5 Hz to 350 MHz</td>
</tr>
<tr>
<td></td>
<td>54642A/D: 3.5 Hz to 500 MHz</td>
</tr>
<tr>
<td>Calculated Risetime</td>
<td>54621A/D: ~5.8 ns</td>
</tr>
<tr>
<td>(≤0.35 bandwidth)</td>
<td>54622A/D, 54640A: ~3.5 ns</td>
</tr>
<tr>
<td></td>
<td>54641A/D: ~1.0 ns</td>
</tr>
<tr>
<td></td>
<td>54642A/D: ~700 ps</td>
</tr>
<tr>
<td>Single Shot Bandwidth</td>
<td>54621A/D, 54622A/D, 54641A/D, 54642A/D: 50 MHz</td>
</tr>
<tr>
<td></td>
<td>54641A/D: 350 MHz maximum</td>
</tr>
<tr>
<td></td>
<td>54642A/D: 500 MHz maximum</td>
</tr>
</tbody>
</table>

* Denotes Warranty Specifications. All others are typical Specifications are valid after a 10-minute warm-up period and ±0 °C from firmware calibration temperature.
Performance Characteristics (continued)

**Vertical System: Analog Channels (continued)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Range</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: 1 mV/div to 5 V/div</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: 2 mV/div to 5 V/div</td>
</tr>
<tr>
<td><strong>Maximum Input</strong></td>
<td>CAT: 100 Vrms, 100 Vpk, CAT II: 100 Vrms, 200 Vpk</td>
</tr>
<tr>
<td></td>
<td>With 1907C/19074 T/L probe: CAT 500 Vpk, CAT II 1000 Vpk</td>
</tr>
<tr>
<td></td>
<td>5 Vrms/500 µA input</td>
</tr>
<tr>
<td><strong>Offset Range</strong></td>
<td>±5 V on ranges &lt;1 mV/div; ±25 V on ranges 10 mV/div to 100 mV/div; ±100 V on ranges ≥200 mV/div</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: 0</td>
</tr>
<tr>
<td></td>
<td>±5 V on ranges &lt;1 mV/div; ±20 V on ranges 10 mV/div to 200 mV/div; ±5 V on ranges ≥200 mV/div</td>
</tr>
<tr>
<td><strong>Dynamic Range</strong></td>
<td>Lower of ±20 dB or ±32 V from center screen</td>
</tr>
<tr>
<td><strong>Input Resistance</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: 1 MΩ ±1%</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: 1 MΩ ±1%, 100 Ω selectable</td>
</tr>
<tr>
<td><strong>Input Capacitance</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: ~14 pF</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: ~13 pF</td>
</tr>
<tr>
<td><strong>Coupling</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: ac, dc ground</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: ac, dc</td>
</tr>
<tr>
<td><strong>BV Limit</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: ~20 MHz selectable</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: ~25 MHz selectable</td>
</tr>
<tr>
<td><strong>Channel-to-Channel Isolation</strong></td>
<td>5462A/D, 54622A/D, dc to 30 MHz: &gt;41 dB; 80 MHz to max bandwidth: &gt;30 dB</td>
</tr>
<tr>
<td>(with channels at same V/div)</td>
<td>5461A/D, 54642A/D: dc to max bandwidth: &gt;40 dB</td>
</tr>
<tr>
<td><strong>Probes</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: 10.11907C shipped standard for each analog channel</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: 10.11907C shipped standard for each analog channel</td>
</tr>
<tr>
<td><strong>Probe Ø (Agilent/HP and Tek-compatible)</strong></td>
<td>Auto probe sense</td>
</tr>
<tr>
<td><strong>BSDL Tolerance</strong></td>
<td>±2 kV</td>
</tr>
<tr>
<td><strong>Noise Peak-to-Peak</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: 2% full scale or 1 mV, whichever is greater</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: 3% full scale or 3 mV, whichever is greater</td>
</tr>
<tr>
<td><strong>Common Mode Rejection</strong></td>
<td>20 dB @ 50 MHz</td>
</tr>
<tr>
<td><strong>DC Vertical Gain Accuracy</strong></td>
<td>±0.0% full scale</td>
</tr>
<tr>
<td><strong>DC Vertical Offset Accuracy</strong></td>
<td>5462A/D, 54622A/D, 5464A/A: 2% full scale or 1 mV, whichever is greater</td>
</tr>
<tr>
<td></td>
<td>5461A/D, 54642A/D: 3% full scale or 3 mV, whichever is greater</td>
</tr>
<tr>
<td><strong>Single Cursor Accuracy</strong></td>
<td>±(DC Vertical Gain Accuracy + DC Vertical Offset Accuracy + 0.2% full scale)</td>
</tr>
<tr>
<td></td>
<td>Example: For 50 mV signal, scope set to 10 mV/div (500 mV full scale), 5 mV offset, accuracy = ±2% (89 mV) + 0.1 (10 mV) + 0.05 (5 mV) + 0.2% (80 mV) = ±3.78 mV</td>
</tr>
<tr>
<td><strong>Dual Cursor Accuracy</strong></td>
<td>±(DC Vertical Gain Accuracy + 0.4% full scale)</td>
</tr>
<tr>
<td></td>
<td>Example: For 50 mV signal, scope set to 10 mV/div (600 mV full scale), 5 mV offset, accuracy = ±2% (80 mV) + 1.4% (10 mV) = ±0.92 mV</td>
</tr>
</tbody>
</table>

---

1. Denotes Warranted Specifications, all others are typical. Specifications are valid after a 30-minute warm-up period and ±10 °C from firmware calibration temperature.
2. For 5462A/D, 54622A/D, 5464A/A, and 54642A/D, 1 mV/div is a magnification of 2 mV/div setting for vertical accuracy calculations, use full scale of 10 mV for 1 mV/div sensitivity setting.
3. For 5461A/D, 5464A/D, and 54642D, 1 mV/div is a magnification of 4 mV/div setting for vertical accuracy calculations, use full scale of 32 mV for 2 mV/div sensitivity setting.
Agilent 33120A
Function/Arbitrary Waveform Generator
Data Sheet

- 15 MHz sine and square wave outputs
- Sine, triangle, square, ramp, noise and more
- 12-bit, 40 MSa/s, 16,000-point deep arbitrary waveforms
- Direct digital synthesis for excellent stability

Uncompromising performance for standard waveforms
The Agilent Technologies 33120A Function/Arbitrary Waveform Generator uses direct digital-synthesis techniques to create a stable, accurate output signal for clean, low-distortion sine waves. It also gives you fast rise- and fall-time-square wave, and linear ramp waveforms down to 100 µHz.

Custom waveform generation
Use the 33120A to generate complex custom waveforms such as a heartbeat or the output of a mechanical transducer. With 12-bit resolution, and a sampling rate of 40 MSa/s, the 33120A gives you the flexibility to create any waveform you need. It also lets you store up to four 16,000-point waveforms in nonvolatile memory.

Easy-to-use functionality
Front-panel operation of the 33120A is straightforward and intuitive. You can access any of ten major functions with a single key press or two, then use a simple knob to adjust frequency, amplitude and offset. To save time, you can enter voltage values directly in Vpp, Vrms or dBm.

Internal AM, FM, FSK and burst modulation make it easy to modulate waveforms without the need for a separate modulation source. Linear and log sweeps are also built in with sweep rates selectable from 1 ms to 609 s. GPIB and RS-232 interfaces are both standard, plus you get full programmability using SCPI commands.

Optional phase-lock capability
The Option 001 phase lock/TCXO timebase gives you the ability to generate synchronized phase-offset signals. An external clock input/output lets you synchronize with up to three other 33120As or with an external 10-MHz clock.

Option 001 also gives you a TCXO timebase for increased frequency stability. With accuracy of 4 ppm/yr, the TCXO timebase makes a 33120A ideal for frequency calibrations and other demanding applications.

With Option 001, new commands let you perform phase changes on the fly, via the front panel or from a computer, allowing precise phase calibration and adjustment.

Link the Agilent 33120A to your PC
The included Agilent IntuiLink software allows you to easily create, edit, and download complex waveforms using the IntuiLink Arbitrary Waveform Editor. Or you can capture a waveform using IntuiLink Oscilloscope or DMM and send it to the 33120A for output. For programmers, ActiveX components can be used to control the instrument using SCPI commands.

IntuiLink provides the tools to easily create, download, and manage waveforms for your 33120A. To find out more about IntuiLink, visit www.agiletech.com/find/intui link.

The 33120A can also be used in conjunction with the 34970A BenchLink Arb software. This Windows*-based program lets you create and edit waveforms on your PC and download them to the 33120A.
Waveforms

- Standard waveforms: sine, square, triangle, ramp, noise, impulse, exponential rise and fall times, square waves.
- Arbitrary waveform length: 0 to 16,000 points.
- Amplitude resolution: 12 bits (including sign).
- Sample rate: 40 MS/s.
- Non-volatile memory: Four (4) 16,000 waveforms.

Frequency Characteristics

- Sine: 100 kHz to 1 MHz.
- Square: 100 kHz to 100 kHz.
- Triangle: 100 kHz to 100 kHz.
- Ramp: 100 kHz to 100 kHz.
- White noise: 10 MHz bandwidth.
- Resolution: 10 MHz or 10 dB.
- Accuracy: 10 ppm in 10 years, 0.01 ppm in 1 year.
- Temp. Coeff.: < 2 ppm/°C.
- Aging: 0.1 ppm/yr.

Sine Wave Spectral Purity

- Harmonic distortion: < 0.01%.
- Total harmonic distortion: DC to 20 kHz: < 0.001%.
- Phase noise: < 0.001% in 20 kHz band.

Signal Characteristics

- Squarewave: Rise/Fall time: < 10 ns.
- Overload: 1%.
- Asymmetry: 1%.
- Duty cycle: 20% to 80% (to 5 MHz), 40% to 80% (to 15 MHz).
- Triangular ramp: Rise/Fall time: 40 ns (typical).
- Linearity: < 0.1% of full scale.
- Settling time: < 250 ns to 0.5% of final value.
- Jitter: < 5 ns.

Output Characteristics

- Amplitude (into 50Ω): 50 mVpp - 10 Vpp (max).
- Accuracy (at 1 kHz): ± 1% of specified output.
- Flatness (at 1 kHz): ± 1% (± 0.1 dB).
- Flatness (at 10 kHz): ± 15% (± 1.5 dB).
- Flatness (at 1 MHz): ± 2% (± 0.2 dB) Ampl ± 300 mV.
- Flatness (at 15 MHz): ± 3% (± 0.3 dB) Ampl ± 300 mV.
- Output impedance: 50Ω (± 10Ω).
- Offset into 50Ω: ± 5 Vpp ± 0.1%.
- Temperature: ± 5% (± 0.1% dB) per °C.
- Power supply: ± 3% (± 0.1% dB) per °C.
- Ripple: ± 3% (± 0.1% dB) per °C.
- Humidity: ± 3% (± 0.1% dB) per °C.
- Altitude: ± 3% (± 0.1% dB) per °C.
- Temperature range: -40°C to 70°C.
- Humidity range: 5% to 95% RH non-condensing.
- Altitude range: 500 to 10,000 ft.

Sweep Characteristics

- Type: Linear or Logarithmic.
- Direction: Up or Down.
- Frequency range: 10 kHz to 1 MHz.
- Crest factor: 1.5 to 30.
- Trigger: Single, External, or Internal.
- External trigger: FSK/Burst Gate.

System Characteristics

- Configuration time: ≤ 100 ms.
- Function change: ≤ 100 ms.
- Frequency change: ≤ 100 ms.
- Amplitude change: ≤ 100 ms.
- Offset change: ≤ 100 ms.
- Select user: ≤ 100 ms.
- Modulation parameter change: ≤ 100 ms.

FSK Download Times over GPIB

- Arb length: Binary: ≤ 1000 points.
- ASCII length: ASCII: ≤ 1000 points.

Other Features:

[1] 100 mVpp - 20 Vpp into open circuit.
[7] For 400 baud, multiply the download times by two. For 2080 baud, multiply the download times by four, etc.
[8] Time for 1-digit numbers; for 12-digit numbers, multiply the 5-digit numbers by two.
**Option 881 PhaseLock/TCXO Timebase**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timebase Accuracy</strong></td>
<td>&lt; 601 ppm</td>
</tr>
<tr>
<td>Stability</td>
<td>± 1 ppm/°F, ±5°/°C</td>
</tr>
<tr>
<td>Aging</td>
<td>&lt; 2 ppm in first 30 days (continuous operation) 0.1 ppm/month (after first 30 days)</td>
</tr>
<tr>
<td>External Reference Input</td>
<td></td>
</tr>
<tr>
<td>Quality</td>
<td>10 MHz ± 50 Hz</td>
</tr>
<tr>
<td>Lock Range</td>
<td>&gt; 80 dBm to +10 dBm, +25 dBm or 10 Vpp peak input</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 Ω ± 2%, 47 Vpk isolation to earth</td>
</tr>
<tr>
<td>Lock Time</td>
<td>&lt; 2 seconds</td>
</tr>
<tr>
<td>Internal Reference Output</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Frequency</td>
<td>&gt; 1 Vpp into 30 Ω</td>
</tr>
<tr>
<td>Phase Offset Range</td>
<td>± 360° to -360°</td>
</tr>
<tr>
<td>Resolution</td>
<td>0.001°</td>
</tr>
<tr>
<td>Accuracy</td>
<td>25 no</td>
</tr>
<tr>
<td>Trigger Output</td>
<td>5 V zero-going pulse</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>&gt; 2 μs typical</td>
</tr>
<tr>
<td>Faintout</td>
<td>200 mV at detector up to 33100 Hz</td>
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</table>

## General

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Supply</strong></td>
<td>110V/120V/220V/240V ± 10%</td>
</tr>
<tr>
<td><strong>Power Line Frequency</strong></td>
<td>45 Hz to 16 Hz and 300 Hz to 800 Hz</td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>5VA peak (28VA average)</td>
</tr>
<tr>
<td><strong>Operating Environment</strong></td>
<td>0°C to 50°C</td>
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<tr>
<td><strong>Storage Temperature</strong></td>
<td>-40°C to 70°C</td>
</tr>
<tr>
<td>State Storage Memory</td>
<td>Power OFF state automatically saved, 3 User Configurable Stored States</td>
</tr>
<tr>
<td>Interface</td>
<td>IEEE 488 and RS-232 standard</td>
</tr>
<tr>
<td><strong>Language</strong></td>
<td>SCR - 1993, IEEE-488.2 standard</td>
</tr>
<tr>
<td><strong>Dimensions (W x H x D)</strong></td>
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</tr>
<tr>
<td>Bench top</td>
<td>254.4mm x 193.0mm x 374 mm</td>
</tr>
<tr>
<td>Rack mount</td>
<td>212.6mm x 88.5mm x 548.3mm</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>4 kg (8.8 lbs)</td>
</tr>
<tr>
<td><strong>Safety Designed to</strong></td>
<td>UL-1244, CSA 1010, EN61010</td>
</tr>
<tr>
<td><strong>EMC Tested to</strong></td>
<td>MIL-461, MIL-4621, MIL-46221</td>
</tr>
<tr>
<td><strong>Vibration and Shock</strong></td>
<td>MIL-1288, Type II, Class 5</td>
</tr>
<tr>
<td><strong>Acoustic Noise</strong></td>
<td>30 dBa</td>
</tr>
<tr>
<td><strong>Warm-up Time</strong></td>
<td>1 hour</td>
</tr>
<tr>
<td><strong>Warranty</strong></td>
<td>1 year</td>
</tr>
</tbody>
</table>

Ordering Information

Agilent 33120A Function/Ac Generator

Opc. 881 Phase Lock/TCXO Timebase Option
Ordering Information

33128A Function/Arbitrary Waveform Generator

Accessories included
Operating manual, service manual, quick reference guide, IntuiLink connectivity software, test data, and power cord

Options
Ogr. 801 Phase lock/TCXO timebase
Ogr. 106 BenchLink Arb software (34811A)
Ogr. 1CM Rack Mount Kit (34119A)*
Ogr. 916 Extra manual set

Manual language options (please specify one)
ABA US English
AEB German
AEC Spanish
AED French
AEE Japanese
AEZ Italian
AED Taiwanese Chinese
AEI Korean

Accessories
Agilent 34161A Accessory pouch
Agilent 34811A BenchLink Arb software

*For racking two side-by-side, order both items below
Lock-link Kit (F/N 5811-9994)
Flange Kit (F/N 5063-9212)

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(fax) 31 26 547 2200
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(fax) 0800 236 331
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5966-9125EN
### PARTS REQUEST FORM

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<th>DESCRIPTION</th>
<th>QTY</th>
<th>APPROVED BY source</th>
<th>COST EA.</th>
<th>PKG</th>
<th>ORDER NUMBER</th>
</tr>
</thead>
<tbody>
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<td>100ohm</td>
<td>2ea</td>
<td>Mouser</td>
<td>0.01</td>
<td>1/4 watt</td>
<td>ME271-100</td>
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<td>pchtet</td>
<td>IRF9530</td>
<td>1ea</td>
<td>Digkey</td>
<td>1.09</td>
<td>TO220</td>
<td>IRF9530-ND</td>
</tr>
</tbody>
</table>

**NOTE** components should be through hole NOT SMD, SMT. NO SOT, SSOP, TSSOP, etc. We can handle a small number of SOIC Please make sure that the component is in stock before ordering.

**RECVD BY** [Name]  **DATE** [Date]
Lab Experiment 2
Resistors and Resistor Color Bands

Date experiment performed: June 7, 2010
Date Lab Report submitted: June 14, 2010
Student name: Howard T. Russell, Jr.
Student ID: 10
Lab Experiment No. 1  

pn-Junction Diode Characterization

I. Introduction
The purpose of this lab is to gain familiarity with the pn-junction diode which is one of the most common of all semiconductor devices. The experiments involved in this lab address the dc characteristics of the diode and how these characteristics are used to extract its PSPICE model parameters. The theory and equations associated with the pn-junction diode are covered in Chapter 1 of your class notes. Your job in this session is to build, test, and evaluate each of the given test circuits in order to expand your hands-on experience in working with semiconductor devices. For each test circuit, make use of the parts supplied by the GTA, and the DMM and dc power supply located on the lab bench.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
- Diode: 1N4148 (DUT)
- Resistors:
  - 200 (1/2 watt) 2K 20K 200K 2M
  - 330 (1/2 watt) 3.3K 33K 330K
  - 820 (1/2 watt) 8.2K 82K 820K

Instruments:
- Power supply
- Multimeter
  - Agilent E3620A
  - Agilent 34401A

Additional:
- Breadboard
- Tool box
- Hook-up wire

III. Diode DC Measurements and Modeling
The schematic for the diode dc test circuit is shown in Figure 1. This simple circuit is used to obtain the forward biased IV characteristics of the device under test (DUT) by sweeping the current \( I_D \) and measuring the corresponding forward voltage \( V_D \). The DUT in this experiment is the 1N4148 small-signal pn-junction diode which is a standard device in many circuit designs. The diode current is swept by setting the power supply voltage \( V_{ps} \) at a constant value (20V) and changing the resistor \( R_m \) with values spanning 200Ω to 2MΩ to obtain a wide dynamic current range. By measuring the voltage across this resistor (\( V_R \)), \( I_D \) is determined from the VCR equation:

\[
I_D = \frac{V_R}{R_m}
\]

With \( V_R \) and \( R_m \) accurately measured, \( I_D \) is an accurate calculation of the diode current. This calculation allows an indirect yet accurate means to determining the diode current.

1. Measurements:
   (a) At the beginning of the experiment, the GTA will provide a 1N4148 diode and an assortment of resistors.
   (b) Build the test circuit shown in Figure 1 to measure the forward IV characteristics of the 1N4148 diode. A photo of the correct way to build this circuit on a breadboard is shown in Figure 2. Request the GTA to verify your circuit prior to making measurements.
   (c) With the resistors provided by the GTA, measure the variables listed in Table 1 for each value of \( R_m \). Record these values in the first six columns of the table in order to obtain the voltage \( V_D \) versus current \( I_D \) data. (Hint: for neatness, you must record these values in your lab notebook before you transfer them to the printed table. You may redraw the table in Word if you wish.)

2. Data processing:
(a) Use the Windows Excel program to plot your measured data in the form of $I_D$ versus $V_D$. An example of this plot is shown in the IV graph in Figure 3. This is the format typical to display a device IV curve; therefore, copy the style of this graph exactly as shown.

3. Parameter extraction:
   (a) At the beginning of the course, you will be provided a copy of an application note entitled “The SPICE Diode Model”. On pages 62 to 64 of this note, a parameter extraction method labeled “Three-point I-V method” for the calculation of the SPICE diode model parameters $R_S$, $N$, and $I_S$ is explained. These parameters correspond to the diode theory model parameters $r_S$, $\eta$, and $I_S$, respectively. Equations for these parameters are given in (3.36) for $R_S$, (3.37) for $N$, and (3.38) for $I_S$. Apply this method to your measured IV data to extract $r_S$, $\eta$, and $I_S$ for your diode. Show all for your calculations and list the values for these parameters.

4. Playback and comparison:
   (a) For the $I_D$ values in calculated in Table 1, calculate the diode voltage $V_{DC}$ using the extracted parameters $r_S$, $\eta$, and $I_S$ in the diode model equation given as

   $$V_{DC} = \eta V_t \ln \left( \frac{I_D}{I_S} + 1 \right) + r_S I_D$$

   where $V_t$ is the thermal voltage of 26mV. Record these calculated voltage values in the seventh column of the table.
   (b) Use Excel to generate a graph with plots of $V_D$ and $V_{DC}$ versus $I_D$ for a visual comparison of the measured and calculated voltages. Use the graph style and format shown in the example graph in Figure 4.
   (c) Evaluate the results of your parameter extraction by generating the error in percent between the measured diode voltage and the calculated voltage with the measured values as the basis. That is, calculate the percent error from

   $$\varepsilon(\%) = \frac{V_{DC} - V_D}{V_D} \cdot 100\%$$

   Record the errors in the last column where indicated. Finally, generate the error function $E_2$ given in equation (3.35) on page 62 in the above mentioned application note where

   $$E_2 = \varepsilon_1(\%)^2 + \varepsilon_2(\%)^2 + \ldots + \varepsilon_{13}(\%)^2 = \sum_{i=1}^{13} \left( \frac{\varepsilon_i(\%)}{100} \right)^2$$

   Record $E_2$ at the bottom of the table where indicated.
   (d) As stated in the application note, the method that yields the lowest value for $E_2$ produces the most accurate values for the extracted parameter values. Therefore, comment on the accuracy of your extracted parameters from the measured and calculated IV plots and $E_2$ value.

5. Lab report: Your lab report on this section of the lab should consist of the following:
   (a) Table 1 completely filled out.
   (b) Values for the model parameters; show all calculation steps.
   (c) Measured IV plot.
   (d) Measured and calculated IV plots on the same graph.
   (e) A plot of $\varepsilon$ in % versus $I_D$.
   (f) A conclusion and comments on the accuracy of your model.
   (g) An appendix containing copies of pages from your lab notebook containing all data and calculations made during the experiment.
Figure 1
Diode dc test circuit

Figure 2
Correct breadboard layout
Figure 3
Typical measured IV characteristics

<table>
<thead>
<tr>
<th>$R_m$ (Ω) (spec.)</th>
<th>$R_m$ (Ω) (meas.)</th>
<th>$V_{ps}$ (V) (meas.)</th>
<th>$V_R$ (V) (meas.)</th>
<th>$I_D$ (A) (calc.)</th>
<th>$V_D$ (V) (meas.)</th>
<th>$V_{DC}$ (V) (calc.)</th>
<th>$\epsilon$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2M</td>
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</tr>
</tbody>
</table>

$E_2$
Figure 4
Typical measured and calculated IV characteristics
Parameter extraction is defined as the determination of model parameters from actual device data that will produce simulated characteristics accurately representing the device. Successful extraction of model parameters relies on the availability and amount of device data obtained from electrical measurements or from characteristic plots on data sheets. For example, the electrical characteristics of the SPICE diode model are controlled by its parameters [1]. By adjusting these parameters, the characteristics of the model can be made to match precisely the characteristics of a real diode. Parameter extraction is therefore the intelligent adjustment of parameters that will allow this precision. The set of parameters which produces the highest degree of simulated accuracy or precision is called the optimal set.

There are many mathematical methods which can be applied to a device model for the extraction of its parameters. In most cases, the complexity of the model, the number \( m \) of model parameters, and the number \( n \) of sampled data points are considered in the method selection. General parameter extraction methods range from simple to complex and are divided into the following groups.

(a.) **Direct solution methods.** With these methods, the parameters are calculated directly from a set of equations derived from the model. These equations involve non-iterative or closed-form solutions, and require a number of data points equal to the number of parameters; that is \( n = m \). Parameters extracted with these methods are not necessarily optimal but can be used as starting or initial values for more complex methods.

(b.) **Data or curve fitting methods.** These consist of regression methods which fit data to model equations represented by straight lines, logarithmic curves, exponential curves, power curves, or polynomial curves [2-6]. The Gram-Schmidt method can be used to fit data with rational functions [7]. The best results in determining optimal parameters are produced when the number of data points exceeds the number of parameters. A proposed rule of thumb is to have at least twice as many data points as parameters; that is, \( n = 2m \) [8].

(c.) **Iterative methods.** These methods employ iterative techniques to solve a set of non-linear equations represented by a Taylor-series expansion. One of these is the least-squares Taylor-Series method which truncates the series after the first derivative [9, 10]. The derivatives are generated directly or approximated with finite differences. For these methods to work efficiently, \( n \) must be greater than twice \( m \), and initial parameter values must be used to start the process. For \( n = m \), the Taylor-Series method simplifies to the generalized Newton-Raphson method [11].

(d.) **Optimization methods.** A few of the most powerful and widely-used of these are the steepest-descent method [12], the Fletcher-Powell method [13], and the Levenberg-Marquart method [14]. These methods also employ iterative solution techniques, and work very well to provide optimal solutions on systems of multi-parameter, non-linear equations used in transistor models, for example. However, the convergence to the set of optimal parameters depends very much on initial parameter values.

Most of these methods use the differences between the device and model data to establish criteria for comparing the various parameter solutions to determine the optimal set. These data differences are called errors and the criteria derived from these errors is called the error criteria. These quantities are illustrated in Figure 1 which represents the hypothetical characteristic curves of a device and its model. The solid
curve labeled \( y_d(x) \) is the device data measured at each of the \( n \) independent variables \( x_1 \) to \( x_n \). The dashed curve labeled \( y_m(x) \) is the calculated data produced by the model over the same range of \( x \). The model data is calculated from

\[
y_m(x) = f_{\text{model}}(x, p)
\]

(1)

where \( f_{\text{model}} \) is a function consisting of the model equations, and \( p \) is an \( m \)-element vector of model parameters. For example, these curves could be the large-signal dc V-I characteristics of a typical diode. In this case, the \( x \)-axis corresponds to the diode current, the \( y \)-axis corresponds to the diode voltage, \( f_{\text{model}}(x, p) \) is the large-signal dc model equation for the SPICE diode, and \( p \) is a 3-element vector containing the parameters IS, N, and RS. At each of the \( x_i \) points, the normalized difference between the data of the device and model is defined as the error \( \varepsilon_i \) where

\[
\varepsilon_i = \frac{y_m(x_i) - y_d(x_i)}{y_d(x_i)} = \frac{f_{\text{model}}(x_i, p) - y_d(x_i)}{y_d(x_i)}
\]

(2)

for \( i = 1 \) to \( n \). The error vector \( \varepsilon \) is defined as a vector containing these errors as its elements. That is,

\[
\varepsilon = \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \vdots \\ \varepsilon_n \end{bmatrix}
\]

(3)

There are several well-known error criteria which can be formulated from the individual errors \( \varepsilon_i \). The criterion commonly used in most extraction methods is the norm of \( \varepsilon \) which is called the error function \( E_2 \). This scalar function is calculated from
The purpose of the methods described above is to minimize the value of $E_2$ which guarantees that errors $\varepsilon_i$ are also minimized. Therefore, the set of extracted parameters which produce the smallest value of $E_2$ is considered to be the optimal set and will provide the most accurate simulation of the device.

There are two basic approaches that can be taken when extracting parameters [15]. The first is called the sequential approach which applies to the extraction of parameters one at a time or in small groups. The second is called the simultaneous approach in which all parameters are extracted in one operation. Obviously, there are considerations for, and advantages and disadvantages to each approach.

The sequential approach involves the extraction of parameters having a dominant effect on an individual characteristic of the device. Therefore, it is important to understand how the parameters are coupled and interact in the simulation of all of the device’s characteristics. For instance, it is known that the parameters IS, N, and RS control the large-signal dc characteristics of the SPICE diode model. Similarly, the reverse-bias junction capacitance characteristics are controlled by the parameters CJO, VJ, M, and FC. Based on the nature of the equations used in this model, these two sets of parameters are decoupled and do not interact. That is, any change in IS, N, or RS has no effect on the reverse-bias C-V characteristics, and vice-versa for any change in CJO, VJ, M, or FC on the large-signal I-V characteristics. Due to this decoupling, the two sets of parameters can be extracted separately without adverse effect on each other's characteristic. Conversely, the parameters IS, N, EG, and XTI are dominant in controlling the temperature characteristics of IS. This characteristic is coupled to the large-signal I-V characteristic because of the commonality or interaction of the two parameters IS and N between the two parameter sets. This coupling must be considered in the extraction of these parameters from the two characteristics.

One of the main advantages to the sequential approach is that each of the device’s characteristics is modeled separately. This permits the extraction process to be broken up into individual subprocesses where different and more efficient extraction methods may be applied. Attention is focused and intuition gained on the particular characteristic being modeled. Another advantage involves the use of simple extraction methods which can be implemented on scientific calculators.

The disadvantage to this approach lies in parameter interaction. Parameters extracted from one characteristic region of operation are assumed constant for another region of operation, and are used to extract other parameters. This causes a non-simultaneous realization of the complete device model such that some characteristics are modeled more accurately than others. Thus, it becomes necessary to specify which characteristics are more important than others so that trade-offs can be applied to resolve the accuracy conflicts.

By extracting all model parameters in one simultaneous operation, the problems of parameter coupling and interaction are more proficiently handled than with the sequential approach. Optimization methods can be very efficiently applied to the simultaneous approach by offering advantages of faster parameter extraction and increased probability of producing an optimal parameter set for the complete model.

There are, however, several disadvantages to the simultaneous approach. First, any insight into the simulation of individual device characteristics is not as clear as with the sequential approach. Second, the general weakness inherent in all optimization methods is the lack of assurance that the method will converge to the absolute or global optimal solution rather than to the nearest or local solution. This weakness can be overcome by providing starting values for the parameters which are close to the optimal solutions. Third, optimization methods involve complex iterative mathematical algorithms. Consequently, computer implementation is required for these methods to enhance the speed and efficiency of the algorithms.

A third approach can be taken which includes the features of these two approaches. The sequential approach is applied first to provide an estimation or approximation of parameter values. These serve as starting values for the simultaneous approach which is applied next to “fine tune” the parameters to their
optimal values. This hybrid approach circumvents some of the disadvantages found in the other two and can be very effective in parameter extraction.

References
5. B. Miller, "Curve fitting made easy", *RF Design*, vol. 13, No. 6, June 1990, pp. 27 to 32.
Lab Experiment No. 2

Diode Applications I

I. Introduction
Diodes have many applications in electronic circuits among which involve converting ac signals into dc levels (known as rectification) and signal clamping and clipping. In this experiment, you will design, build, and examine the operation of two well-known rectifier circuits that use diodes. These circuits are found in the front end of many linear dc power supplies. In addition, you will build and examine how diodes are used in the processing of various signals in circuits designed to clip and steer voltages and currents. These circuits are functional in many signal shaping and conditioning applications. Download the data sheet for the small-signal junction diode 1N4148. You will need this document for the diode pin configuration and maximum ratings. For each of the circuits listed in this experiment, make use of the parts supplied by the GTA, and the equipment located on the lab bench.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:

- **Diode**:
  - 1N4148 (4)
- **Resistors**:
  - 1K
- **Capacitors**:
  - 0.1μF
  - 1.0μF
  - 50μF

Instruments:

- **Power supply**: Agilent E3620A
- **Multimeter**: Agilent 34401A
- **Function generator**: Agilent 33120A
- **Oscilloscope**: Agilent 54621A

Additional:
- Breadboard
- Tool box
- Hook-up wire

III. Half-Wave Rectifier Analysis and Measurement
The schematic for a half-wave rectifier is shown in Figure 1 where the filter capacitor $C_L$ is left as a variable. Build this circuit on your breadboard with the Agilent function generator for $E_g(t)$ and do the following:

(a) Draw as accurately as possible on quadrille graph paper the time-domain waveforms for $E_g(t)$ and $V_o(t)$ with $C_L = 0$, 0.1μF, and 50μF. For each value of $C_L$, locate these waveforms close to each other so they can be easily compared. Clearly label the peak values and periods of the waveforms.

(b) Accurately fill out Tables 1 and 2 with data taken from circuit analysis calculations and circuit measurements.
Table 1
Half-wave rectifier output with $C_L = 0$

<table>
<thead>
<tr>
<th>$V_o(t)$</th>
<th>Calculated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dc (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rms (V)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2
Half-wave rectifier output with variable $C_L$

<table>
<thead>
<tr>
<th>$V_o(t)$</th>
<th>$C_L = 0.1\mu F$</th>
<th>$C_L = 50\mu F$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Calculated</td>
<td>Calculated</td>
</tr>
<tr>
<td></td>
<td>Measured</td>
<td>Measured</td>
</tr>
<tr>
<td>dc (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple factor (%)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IV. Half-Wave Rectifier Design

Design a half-wave rectifier that will meet the following specifications:
(a) $E_g(t)$ with a peak voltage of 8V and a sinusoidal frequency of 400Hz.
(b) A dc output voltage of 5V.
(c) The least valued filter capacitor $C_L$ that will produce a maximum ripple voltage of 100mV.

Neatly draw the schematic of your design with the values of all components clearly labeled. Verify that your design meets the above specifications by filling out Tables 3 and 4 with calculated and measured data.

Table 3
Half-wave rectifier design with $C_L = 0$

<table>
<thead>
<tr>
<th>$V_o(t)$</th>
<th>Calculated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dc (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rms (V)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
V. Full-Wave Rectifier Analysis and Measurement
The schematic for a full-wave rectifier is shown in Figure 2 where the filter capacitor $C_L$ is left as a variable. Build this circuit on your breadboard with the Agilent function generator for $E_g(t)$ and do the following:
(a) Draw as accurately as possible on quadrille graph paper the time-domain waveforms for $E_g(t)$ and $V_o(t)$ with $C_L = 0$, $0.1 \mu F$, and $50 \mu F$. For each value of $C_L$, locate these waveforms close to each other so they can be easily compared. Clearly label the peak values and periods of the waveforms.
(b) Accurately fill out Tables 5 and 6 with data taken from circuit analysis calculations and circuit measurements.

Figure 2
Full-wave rectifier

Table 4
Half-wave rectifier design with $C_L$

<table>
<thead>
<tr>
<th>$V_o(t)$</th>
<th>Calculated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple factor (%)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5
Full-wave rectifier output with $C_L = 0$

<table>
<thead>
<tr>
<th>$V_o(t)$</th>
<th>Calculated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dc (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rms (V)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
VI. Full-Wave Rectifier Design
Design a full-wave rectifier that will meet the following specifications:
(a) $E_g(t)$ with a peak voltage of 8V and a sinusoidal frequency of 400Hz.
(b) A dc output voltage of 5V.
(c) The least valued filter capacitor $C_L$ that will produce a maximum ripple voltage of 100mV.
Neatly draw the schematic of your design with the values of all components clearly labeled. Verify that your design meets the above specifications by filling out Tables 7 and 8 with calculated and measured data.

<table>
<thead>
<tr>
<th>$V_o(t)$</th>
<th>$C_L = 0.1\mu F$</th>
<th>$C_L = 50\mu F$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Calculated</td>
<td>Measured</td>
</tr>
<tr>
<td>dc (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple factor (%)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6
Full-wave rectifier output with variable $C_L$

Table 7
Full-wave rectifier design with $C_L = 0$

Table 8
Full-wave rectifier design with $C_L$

VII. Voltage Clipper
The schematic for a double voltage clipper circuit is shown in Figure 3 where the power supply voltages $V_{psp}$ and $V_{psn}$ are left as variables. Build this circuit on your breadboard with the Agilent function generator for $E_g(t)$ and do the following:
(a) Draw as accurately as possible on quadrille graph paper the time-domain waveforms for $E_g(t)$ and $V_o(t)$ with $V_{psp}$ and $V_{psn}$ both equal to 5V. Clearly label the peak values and periods of the waveforms.
(b) Repeat part (a) with $V_{psp} = V_{psn} = 9V$.
(c) Explain any differences between the waveforms for $V_o(t)$ observed in parts (a) and (b).
(d) Explain any useful applications this circuit may have. Be specific.

\[ V_{o}(t) = 10\text{V}\sin(2\pi 1000t) \]

VIII. Logic Gates
Diodes can be applied in the design of digital logic gates. The circuit shown in Figure 4(a) is an AND gate while the one in Figure 4(b) is an OR gate. Build these circuits on your breadboard with the Agilent power supply for inputs \( E_1 \) and \( E_2 \), and supply voltage \( V_{psp} \), and do the following:

(a) With 5V as the logic ‘1’ state and 0V as the logic ‘0’ state for inputs \( E_1 \) and \( E_2 \), apply these voltages to the gates in Figure 4(a) and (b). Measure the output voltage \( V_o \) and fill out the truth table in Table 9 for the AND gate and the truth table in Table 10 for the OR gate.

(b) From the voltage data in these tables, define the noise margins for each gate.
### Table 9
AND gate truth table

<table>
<thead>
<tr>
<th>$E_1$</th>
<th>$E_2$</th>
<th>$V_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volts</td>
<td>State</td>
<td>Volts</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>5</td>
</tr>
</tbody>
</table>

### Table 10
OR gate truth table

<table>
<thead>
<tr>
<th>$E_1$</th>
<th>$E_2$</th>
<th>$V_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volts</td>
<td>State</td>
<td>Volts</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>5</td>
</tr>
</tbody>
</table>

IX. Lab Report
Your lab report on this experiment should contain the following:
(a) Drawings of all waveforms for the rectifier circuits.
(b) Equations and calculations from analysis of the given circuits.
(c) Explanations of the operations of each circuit.
(d) Detailed explanation of any differences between calculations and measurements. Be sure to account for the forward voltage of the diode.
(e) Any applications of these circuits- good or bad.
Lab Experiment No. 3

I. Introduction
In addition to applications in rectifiers and clippers, diodes are applied in voltage multiplier networks. As the name implies, voltage multipliers increase a given dc voltage to a value many times its original value through a charge transfer procedure. Diodes are employed as switches in this procedure to enable charge to be transferred among capacitors to increase their voltage. Voltage multipliers are used in many high-voltage, low-current circuits such as Geiger counters, fluorescent lamps, and cathode ray tubes. Your job in this session is to build, test, and evaluate two voltage multipliers (one that doubles a voltage and one that quadruples a voltage) in order to expand your hands-on experience working with these circuits. For each circuit, make use of the parts supplied by the GTA, and the equipment located on the lab bench.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:

<table>
<thead>
<tr>
<th>Component</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>1N4148 (4)</td>
</tr>
<tr>
<td>Resistors</td>
<td>330KΩ, 820KΩ, 1.0MΩ, 3.3MΩ, 4.7MΩ</td>
</tr>
<tr>
<td>Capacitors</td>
<td>10nF (4), 0.1µF (4)</td>
</tr>
</tbody>
</table>

Instruments:

<table>
<thead>
<tr>
<th>Instrument</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>Agilent E3620A</td>
</tr>
<tr>
<td>Multimeter</td>
<td>Agilent 34401A</td>
</tr>
<tr>
<td>Function generator</td>
<td>Agilent 33120A</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Agilent 54621A</td>
</tr>
</tbody>
</table>

Additional:

- Breadboard
- Tool box
- Hook-up wire

III. Voltage Doubler
The schematic of a diode applied voltage doubler is shown in Figure 1. Build this circuit on your breadboard. Connect the function generator for the input voltage $E_g(t)$ and connect the DMM to measure the dc voltage $V_o$.

(a) With an open circuit for the load resistor $R_L$ ($R_L = \infty$), set the function generator to a sine wave and fill out Table 3.1 with measured values for $V_o$ as functions of the peak value $E_m$ and frequency $f$ where

\[ E_g(t) = E_m \sin(2\pi ft) \]

\[ E_m = \text{peak voltage (V)} \]

\[ f = \text{frequency (Hz)} \] (1)

(b) With an open circuit for the load resistor $R_L$ ($R_L = \infty$), set the function generator to a square wave and fill out Table 3.2 with measured values for $V_o$ as functions of the peak value $E_m$ and frequency $f$ of the square wave.

(c) With the function generator set to an 8V, 3KHz sine wave, fill out Table 3.3 with measured values for $V_o$ and load current $I_L$ as functions of the load resistor $R_L$. 

- 48 -
Figure 1
Voltage doubler

Table 3.1
Voltage doubler, sine wave input, $R_L = \infty$

<table>
<thead>
<tr>
<th>$E_m$ (V)</th>
<th>Theoretical $V_o$ (V)</th>
<th>Measured $V_o$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$f = 100\text{Hz}$</td>
</tr>
<tr>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2
Voltage doubler, square wave input, $R_L = \infty$

<table>
<thead>
<tr>
<th>$E_m$ (V)</th>
<th>Theoretical $V_o$ (V)</th>
<th>Measured $V_o$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$f = 100\text{Hz}$</td>
</tr>
<tr>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 3.3
Voltage doubler, 8V, 3KHz sine wave input

<table>
<thead>
<tr>
<th>R_L (Ω)</th>
<th>V_o (V)</th>
<th>I_L (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.3M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>820K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>330K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IV. Voltage Quadrupler

The schematic of a diode applied voltage quadrupler is shown in Figure 2. Build this circuit on your breadboard. Connect the function generator for the input voltage $E_g(t)$ and connect the DMM to measure the dc voltage $V_o$.

(a) With an open circuit for the load resistor $R_L (R_L = \infty)$, set the function generator to a sine wave and fill out Table 3.4 with measured values for $V_o$ as functions of the peak value $E_m$ and frequency $f$ where

$$E_g(t) = E_m \sin(2\pi ft)$$

$$E_m = \text{peak voltage (V)}$$

$$f = \text{frequency (Hz)}$$

(b) With an open circuit for the load resistor $R_L (R_L = \infty)$, set the function generator to a square wave and fill out Table 3.5 with measured values for $V_o$ as functions of the peak value $E_m$ and frequency $f$ of the square wave.

(c) With the function generator set to an 8V, 3KHz sine wave, fill out Table 3.6 with measured values for $V_o$ and load current $I_L$ as functions of the load resistor $R_L$.

\[D_1 - D_4 - 1N4148\]
\[C_1 - C_4 - 0.1\mu F\]

Figure 2
Voltage quadrupler
### Table 3.4
Voltage quadrupler, sine wave input, $R_L = \infty$

<table>
<thead>
<tr>
<th>$E_m$ (V)</th>
<th>Theoretical $V_o$ (V)</th>
<th>Measured $V_o$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$f$ = 100Hz</td>
</tr>
<tr>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

|          |                      | $f$ = 1KHz          |
| 2.0      |                       |                     |
| 4.0      |                       |                     |
| 6.0      |                       |                     |
| 8.0      |                       |                     |
| 10.0     |                       |                     |

|          |                      | $f$ = 10KHz         |
| 2.0      |                       |                     |
| 4.0      |                       |                     |
| 6.0      |                       |                     |
| 8.0      |                       |                     |
| 10.0     |                       |                     |

### Table 3.5
Voltage quadrupler, square wave input, $R_L = \infty$

<table>
<thead>
<tr>
<th>$E_m$ (V)</th>
<th>Theoretical $V_o$ (V)</th>
<th>Measured $V_o$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$f$ = 100Hz</td>
</tr>
<tr>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

|          |                      | $f$ = 1KHz          |
| 2.0      |                       |                     |
| 4.0      |                       |                     |
| 6.0      |                       |                     |
| 8.0      |                       |                     |
| 10.0     |                       |                     |

|          |                      | $f$ = 10KHz         |
| 2.0      |                       |                     |
| 4.0      |                       |                     |
| 6.0      |                       |                     |
| 8.0      |                       |                     |
| 10.0     |                       |                     |

### Table 3.6
Voltage quadrupler, 8V, 3KHz sine wave input

<table>
<thead>
<tr>
<th>$R_L$ (Ω)</th>
<th>$V_o$ (V)</th>
<th>$I_L$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.3M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>820K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>330K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
V. Lab Report

Your lab report on this experiment should contain the following:

(a) Detailed explanation of how the voltage doubler works. Give reasons for any deviations from expected results for the output voltage $V_o$.

(b) Explanation of differences between theoretical and measured values for $V_o$ with no load. Does the type of waveform (sine wave vs. square wave), frequency, or amplitude affect $V_o$? If so, explain why.

(c) Explanation of differences between theoretical and measured values for $V_o$ with load. Does the type of waveform (sine wave vs. square wave), frequency, or amplitude affect $V_o$? If so, explain why.

(d) Does the forward voltage drop of the diode affect $V_o$? Explain why or why not.

(e) Explain how a voltage multiplier such as the ones studied in this experiment can be applied to generate a negative voltage. Provide a schematic to illustrate this application.
Lab Experiment No. 4  

BJT Device Characterization

I. Introduction
The purpose of this lab is to gain familiarity with the NPN bipolar junction transistor (BJT), and the PNP BJT. The experiments involved in this lab address the dc characteristics of the devices and how these characteristics are used in modeling the devices. The theory and equations associated with these devices are covered in Chapter 1 of your class notes. Your job in this session is to build, test, and evaluate each of the given test circuits in order to expand your hands-on experience in working with semiconductor devices. For each test circuit, make use of the parts supplied by the GTA, and the DMM and dc power supply located on the lab bench.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
- NPN and PNP measurement circuits
  - Op-amp: OP-07
  - NPN: 2N3904 (DUT)
  - PNP: 2N3906 (DUT)
- Capacitors: 220pF (2)
- Resistors: 51 (1/2 watt) 82 (1/2 watt) 200 510 820
  - 2K (2) 3K 5.1K 8.2K (2) 20K (2)
  - 30K 51K 82K 200K (3) 300K 820K 2M

Instruments:
- Power supply
- Multimeter
  - Agilent E3620A
  - Agilent 34401A

Additional:
- Breadboard
- Tool box
- Hook-up wire

III. NPN BJT Gummel Measurements
The schematic for an NPN BJT dc test circuit is shown in Figure 1. This circuit is the basis for the stimulus-measurement unit (SMU) employed in semiconductor parameter analyzers (SPA) such as the HP4145 or newer Agilent 4142. Its application of the OP-07 operational amplifier allows the collector current \(I_C\) of the NPN BJT DUT to be varied while maintaining a constant collector-emitter voltage \(V_{CE}\). With \(I_C\) swept over a wide dynamic range, the base current \(I_B\) and the base-emitter voltage \(V_{BE}\) are measured and graphed for display of the Gummel plots \((I_C \text{ versus } V_{BE})\) and the \(\beta\) characteristics \((\beta \text{ versus } I_C)\). These plots are very important in BJT characterization and modeling. In the circuit shown below, the voltage at the op-amp’s negative input terminal \((V_n)\) is fixed at 5V by the voltage divider \(R_1\) and \(R_2\). Since the op-amp forces this voltage to be mirrored at its positive input terminal \((V_p = V_n)\), then \(V_{CE}\) of the DUT is also fixed at 5V. The OP-07 employs an input bias current cancellation scheme such that the currents into the positive and negative input terminals are very small and have no effect on the DUT currents. Therefore, the DUT’s collector current is set by the resistor \(R_C\) where

\[
I_C = \frac{V_C}{R_C} = \frac{V_{op} - V_p}{R_C} \quad (1)
\]

The base current is determined by measuring the voltage across \(R_B\) so that

\[
I_B = \frac{V_B}{R_B} \quad (2)
\]

- 53 -
For typical values of \( \beta \), \( I_B \) can be on the order of nano-amps (\text{nA}) to micro-amps (\text{\( \mu \)A}). This suggests that \( R_B \) should be in the range of 100\( \Omega \) to 10\( \Omega \) to allow precise measurements for \( V_B \). The results from these two equations are combined to calculate the DUT \( \beta \) measured at the dc bias condition specified by \( I_C \) and \( V_{CE} \); that is

\[
\beta = \frac{I_C}{I_B} \frac{I_C}{I_{C, V_C}} \tag{3}
\]

The base-emitter voltage is easily measured at the corresponding DUT terminals. Finally, a compensation capacitor \( C_c \) is connected between the output and negative input terminals to insure circuit stability by preventing unwanted oscillations.

1. Measurements:
   (a) At the beginning of the experiment, the GTA will provide you a 2N3904 NPN BJT and an assortment of resistors.
   (b) Build the test circuit shown in Figure 1 to measure the forward Gummel characteristics of the 2N3904. A photo of the correct way to build this circuit on a breadboard is shown in Figure 2. Request the GTA to verify your circuit prior to making measurements.
   (c) With the resistors provided by the GTA, measure the variables listed in Tables 1(a) and 1(b) for specified values of \( R_C \) and \( R_B \). Record these values in the table in order to obtain the Gummel characteristics.
      (Hint: for neatness, you must record these values in your lab notebook before you transfer them to the printed table. You may redraw the tables in Word if you wish.)

2. Data processing:
   (a) Use the Windows Excel program to plot your measured data in the form of
      (i.) \( I_C \) and \( I_B \) versus \( V_{BE} \) for the Gummel plot (typical plot shown in Figure 3), and
      (ii.) \( \beta \) versus \( I_C \) for the forward \( \beta \) plot (typical plot shown in Figure 4).
      Copy the style of the example graphs exactly as shown.

3. Lab report: Your lab report on this section of the lab should consist of the following:
   (a) Tables 1(a) and 1(b) completely filled out.
   (b) Measured Gummel and \( \beta \) plots.
   (c) A conclusion and comments on the accuracy of your measurements.
   (d) An appendix containing copies of pages from your lab notebook containing all data and calculations made during the experiment.

- 54 -
**Figure 2**
Correct breadboard layout

<table>
<thead>
<tr>
<th>Table 1(a)</th>
<th>2N3904 measurements</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_C$ (spec.)</td>
<td>51KΩ</td>
</tr>
<tr>
<td>$R_B$ (spec.)</td>
<td>2MΩ</td>
</tr>
<tr>
<td>$R_C^*$</td>
<td></td>
</tr>
<tr>
<td>$R_B$</td>
<td></td>
</tr>
<tr>
<td>$V_{pp}$</td>
<td></td>
</tr>
<tr>
<td>$V_{psn}$</td>
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</tr>
<tr>
<td>$V_n$</td>
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</tr>
<tr>
<td>$V_p$ ($V_{CE}$)</td>
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</tr>
<tr>
<td>$V_C$</td>
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<tr>
<td>$I_C$</td>
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<td>$V_o$</td>
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<td>$V_B$</td>
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<td></td>
</tr>
<tr>
<td>$\beta$</td>
<td></td>
</tr>
</tbody>
</table>

- 55 -
* Measured values of these variables.

<table>
<thead>
<tr>
<th>Table 1(b)</th>
<th>2N3904 measurements</th>
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<td></td>
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<td>820Ω</td>
</tr>
<tr>
<td>R_C</td>
<td>82Ω</td>
</tr>
<tr>
<td>R_B</td>
<td>30KΩ</td>
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<td></td>
</tr>
<tr>
<td>V_ps</td>
<td></td>
</tr>
<tr>
<td>V_n</td>
<td></td>
</tr>
<tr>
<td>V_p (V_CE)</td>
<td></td>
</tr>
<tr>
<td>V_C</td>
<td></td>
</tr>
<tr>
<td>I_C</td>
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</tr>
<tr>
<td>V_o</td>
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<tr>
<td>V_B</td>
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<tr>
<td>I_B</td>
<td></td>
</tr>
<tr>
<td>V_BE</td>
<td></td>
</tr>
<tr>
<td>β</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3
Typical Gummel plot
IV. PNP BJT Gummel Measurements

The schematic for an PNP BJT dc test circuit is shown in Figure 5. Build this test circuit on your breadboard, and repeat the measurement and data processing procedure described for the 2N3904 NPN for a 2N3906 PNP. Reproduce the data tables (Tables 2(a) and 2(b)) and graphs for the Gummel and $\beta$ plots for this device. Generate an identical lab report for this section of the experiment describing the measurements taken from the 2N3906.

![Figure 5](image_url)  
**Figure 5**  
PNP BJT Gummel test circuit
<table>
<thead>
<tr>
<th>RC (spec.)</th>
<th>51kΩ</th>
<th>20kΩ</th>
<th>8.2kΩ</th>
<th>5.1kΩ</th>
<th>2kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>RB (spec.)</td>
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<td>820kΩ</td>
<td>300kΩ</td>
<td>200kΩ</td>
<td>82kΩ</td>
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</table>

<table>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
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</tr>
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<td>V_{psp}</td>
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<td>V_{psn}</td>
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<tr>
<td>V_{n}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{p (V_{CE})}</td>
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<tr>
<td>V_{C}</td>
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<td></td>
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<td>I_{C}</td>
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<tr>
<td>V_{BE}</td>
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<td></td>
</tr>
<tr>
<td>β</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Table 2(b)</td>
<td>2N3906 measurements</td>
<td></td>
<td></td>
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<tr>
<td>------------</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>R_C (spec.)</td>
<td>82Ω  510Ω  200Ω  82Ω  51Ω</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_B (spec.)</td>
<td>30KΩ  20KΩ  8.2KΩ  3KΩ  2KΩ</td>
<td></td>
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<tr>
<td>R_C^*</td>
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<td></td>
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<tr>
<td>R_B</td>
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<tr>
<td>V_psp</td>
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<tr>
<td>V_psn</td>
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<tr>
<td>V_n</td>
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<td></td>
</tr>
<tr>
<td>V_p (V_CE)</td>
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<td></td>
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<tr>
<td>V_C</td>
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<td></td>
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<tr>
<td>I_C</td>
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<tr>
<td>V_o</td>
<td></td>
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<tr>
<td>V_B</td>
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<tr>
<td>I_B</td>
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<td></td>
</tr>
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<td>V_BE</td>
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<td></td>
</tr>
<tr>
<td>β</td>
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</tbody>
</table>
I. Introduction
The purpose of this lab is to gain familiarity with MOSFET devices. The experiments involved in this lab address the forward dc transfer characteristics of n-channel and p-channel devices and how these characteristics are used in device modeling. The theory and equations associated with these devices are covered in a class handout. Your job in this session is to build, test, and evaluate each of the given test circuits in order to expand your hands-on experience working with MOSFETs. For each test circuit, make use of the parts supplied by the GTA, and the DMM and dc power supply located on the lab bench.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
- MOS measurement circuits –
  - Op-amp: OP-07 (2)
  - n-ch: ALD1103/n-ch
  - p-ch: ALD1103/p-ch
- Capacitors: 220pF (2)
- Resistors: 68 (1/2 watt) 100 (1/2 watt) 200 270 680 2K 6.8K 20K 30K (2) 68K 120K 200K 10K trimpot

Instruments:
- Power supply Agilent E3620A
- Multimeter Agilent 34401A
- Additional:
  - Breadboard
  - Tool box
  - Hook-up wire

III. ENMOS Measurements
The schematic for an enhancement mode, n-channel, MOSFET (ENMOSFET) dc test circuit is shown in Figure 1. This circuit is the basis for the stimulus-measurement unit (SMU) employed in semiconductor parameter analyzers (SPA) such as the HP4145 or newer Agilent 4142. Its application of the OP-07 operational amplifier (OA1) allows the drain current (I_D) of the DUT to be varied while maintaining a constant drain-source voltage (V_DS). With the source-body voltage (V_SB) set to a constant value by a voltage reference circuit and with I_D swept over a wide dynamic range, the gate-source voltage (V_GS) is measured and graphed for display of the forward transfer characteristics plot (I_D versus V_GS and V_SB). This plot is very important in MOSFET characterization and modeling. In the circuit shown below, the voltage at the op-amp’s negative input terminal (V坳) is fixed at 8V by the voltage divider R₁ and R₂. Since the op-amp forces this voltage to be mirrored at its positive input terminal (V_p = V坳), then V_DS of the DUT is also fixed at 8V. Op-amp OA₂ and the 10KΩ trimpot R₇ make up a unity-gain buffer with an adjustable output voltage Vₒ₂ to set the source-body voltage V_SB. The OP-07 employs an input bias current cancellation scheme such that the currents into the positive and negative input terminals of OA₁ are very small and have no effect on the DUT currents. Therefore, the DUT’s drain current is set by the resistor R₀ where

\[ I_D = \frac{V_p}{R_D} = \frac{V_{pp} - V_p}{R_D} \]  

(1)
The model for the drain current $I_D$ in the saturation region is given by

$$I_D = \beta (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$  \hspace{1cm} (2)$$

The gate-source voltage is easily measured at the corresponding DUT terminals. Finally, 220pF compensation capacitors $C_{c1}$ and $C_{c2}$ are connected to OA1 and DUT as indicated to insure circuit stability by preventing unwanted oscillations.

1. **Measurements:**
   (a) At the beginning of the experiment, the GTA will provide you with an ALD1103 and an assortment of resistors.
   (b) Build the test circuit shown in Figure 1 to measure the forward transfer characteristics of one of the n-channel MOSFET on the chip. Request the GTA to verify your circuit prior to making measurements.
   (c) With the resistors provided by the GTA, measure the variables listed in Tables 1(a) and 1(b), and Tables 2(a) and 2(b) for specified values of $R_D$ and $V_{SB}$. Record these values in the tables in order to obtain the transfer characteristics.
   (Hint: for neatness, you must record these values in your lab notebook before you transfer them to the printed table. You may redraw the tables in Word if you wish.)

2. **Data processing:**
   (a) Use the Windows Excel program to plot your measured data in the form of
      (i) $I_D$ versus $V_{GS}$ for the forward transfer characteristics plot for $V_{SB} = 0V$, and
      (ii) $I_D$ versus $V_{GS}$ for the forward transfer characteristics plot for $V_{SB} = 2V$.
   (b) Model parameter extraction (assume $\lambda V_{DS} << 1$)
      (i) extract the threshold voltage $V_{TH}$ and the transconductance parameter $\beta$ from the transfer characteristics data for $V_{SB} = 0V$, and
      (ii) extract the threshold voltage $V_{TH}$ and the transconductance parameter $\beta$ from the transfer characteristics data for $V_{SB} = 2V$.

3. **Lab report:** Your lab report on this section of the lab should consist of the following:
   (a) Tables 1 and 2.
   (b) Measured forward transfer characteristics plots for the two $V_{SB}$ values.
   (c) Extracted $V_{TH}$ and $\beta$ for the two $V_{SB}$ values.
   (d) Calculated forward transfer characteristics plots for the two $V_{SB}$ values (apply the parameters in (c.) to equation (2)).
   (e) A conclusion and comments on the accuracy of your measurements and extracted parameters.
   (f) An appendix containing copies of pages from your lab notebook containing all data and calculations made during the experiment.

---

\[1\] Download the ALD1103 data sheet from the Advanced Linear Devices, Inc. website www.aldinc.com.
IV. EPMOS Measurements
The schematic for a p-channel, enhancement mode MOSFET dc test circuit is shown in Figure 2. Build this test circuit on your breadboard, and repeat the measurement and data processing procedure described for the n-channel MOS for one of the p-channel MOSFETs on the ALD1103 chip. Reproduce the data tables (Tables 3(a) and 3(b), and Tables 4(a) and 4(b)) and the forward transfer characteristics plots for the device. Generate an identical lab report for this section of the experiment describing the measurements taken from the p-channel device.

![Figure 2](image)

**Figure 2**
Forward transfer characteristics test circuit

<table>
<thead>
<tr>
<th>Table 3(a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALD1103/p-ch measurements (V_{BS} = 0V)</td>
</tr>
<tr>
<td>(R_D) (spec.)</td>
</tr>
<tr>
<td>(V_{BS})*</td>
</tr>
<tr>
<td>(R_D)*</td>
</tr>
<tr>
<td>(V_{psp})</td>
</tr>
<tr>
<td>(V_{psn})</td>
</tr>
<tr>
<td>(V_n)</td>
</tr>
<tr>
<td>(V_p (V_{SD}))</td>
</tr>
<tr>
<td>(V_D)</td>
</tr>
<tr>
<td>(I_D)</td>
</tr>
<tr>
<td>(V_{o1})</td>
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<tr>
<td>(V_{SG})</td>
</tr>
</tbody>
</table>

* Measured values of these variables.
### Table 3(b)
**ALD1103/p-ch measurements (V_{BS} = 0V)**

<table>
<thead>
<tr>
<th>R_D (spec.)</th>
<th>680Ω</th>
<th>270Ω</th>
<th>200Ω</th>
<th>100Ω</th>
<th>68Ω</th>
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<tbody>
<tr>
<td>V_{BS}^*</td>
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</table>

* Measured values of these variables.

### Table 4(a)
**ALD1103/p-ch measurements (V_{BS} = 2V)**

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<thead>
<tr>
<th>R_D (spec.)</th>
<th>200KΩ</th>
<th>68KΩ</th>
<th>20KΩ</th>
<th>6.8KΩ</th>
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</thead>
<tbody>
<tr>
<td>V_{BS}^*</td>
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<td>R_D^*</td>
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<td>V_p (V_{SD})</td>
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<td>V_D</td>
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<tr>
<td>V_{o1}</td>
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<tr>
<td>V_{SG}</td>
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</table>

* Measured values of these variables.
<table>
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<th>680Ω</th>
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<th>200Ω</th>
<th>100Ω</th>
<th>68Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{BS}^*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_D^*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{psp}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{psn}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_n</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_p (V_{SD})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{01}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{SG}</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

* Measured values of these variables.
Lab Experiment No. 6  
Self-Biased Current Sinks and Sources

I. Introduction
The purpose of this lab is to evaluate the performance of self-biased dc constant currents sinks and sources known as current regulator diodes [1]. The circuits presented here represent two commonly-used current regulators built with self-biased n and p-channel JFETs. The theory and equations associated with these circuits are covered in class lectures and in the application note attached to this experiment [2]. Your job in this session is to build, test and evaluate each of the given current sink/source circuits in order to expand your hands-on experience in working with these circuits. For each circuit, make use of the parts supplied by the GTA, and the DMM and dc power supply located on the lab bench.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
NJFET: J111 (2)
PJFET: J176 (2)
Resistors:
470 820 1.2K 5.1K 9.1K
10K 15K

Instruments:
Power supply
Multimeter
Agilent E3620A
Agilent 34401A

Additional:
Breadboard
Tool box
Hook-up wire

III. Single-Stage, Source-Biased JFET Current Regulator
The schematic of a single-stage n-channel JFET current sink biased with a resistor in the source is shown in Figure 1. This circuit is known as the single-stage, source-biased JFET current sink. For the device in the saturation region where the drain-source voltage $V_{DS}$ is defined by

$$V_{DS} \leq V_{DS} (sat) = V_p - (V_{GS})$$

(1)

the sink’s output current $I_o$ is identical to $J_1$’s drain current $I_D$ and is expressed as
In these equations, \( V_P \) is the device pinch-off voltage, \( I_{DSS} \) is the drain-source saturation current with the gate shorted to the source and \( \lambda \) is the channel-length modulation parameter in V\(^{-1}\). With the gate shorted to ground, the gate-source voltage is

\[
V_{GS} = -R_S I_o
\]  

(3)

If the source resistor \( R_S \) is known, equations (2) and (3) are combined under the assumption \( \lambda V_{DS} \ll 1 \) to produce a quadratic equation for the output current

\[
I_o^2 \left( \frac{V_P}{R_S} \right)^2 \left( 2 \frac{R_S}{V_P} + \frac{1}{I_{DSS}} \right) I_o + \left( \frac{V_P}{R_S} \right)^2 = 0
\]

(4)

The combination of these two equations represents the intersection of a parabola (equation (2)) with a straight line (equation (3)). Therefore, the solution of this quadratic equation yields two values for \( I_o \) determined from the intersection points. However, only one \( I_o \) value is correct since the other lies outside the valid operating region of the JFET. The value of \( R_S \) that will produce a value for \( I_o \) which will be less than or equal to \( I_{DSS} \) is calculated from

\[
R_S = \frac{V_P}{I_o} \left( 1 - \sqrt{\frac{I_o}{I_{DSS}}} \right)
\]

(5)

If parameters \( \lambda \), \( V_P \), and \( I_{DSS} \) are extracted from device measurements, \( R_S \) is calculated from (5) to produce the desired value for \( I_o \). The small-signal output resistance \( R_o \) of the sink is calculated from

\[
R_o = r_o + R_S \left( 1 + g_{mf} r_o \right)
\]

(6)

In this expression, \( r_o \) is the output resistance of the JFET determined from the slope of the output characteristics curve and \( g_{mf} \) is the forward transconductance. These small-signal bias-dependent components are calculated from

\[
r_o = \frac{1}{\lambda} \frac{V_{DS}}{I_D} = \frac{1 + \lambda V_{DS}}{\lambda I_D} = \frac{1 + \lambda V_{DS}}{\lambda I_o}
\]

(7)

and

\[
g_{mf} = \frac{2 \sqrt{I_{DSS} I_D}}{V_P} = \frac{2 \sqrt{I_{DSS} I_o}}{V_P}
\]

(8)

where \( I_D \) is equal to \( I_o \) as indicated. Finally, the minimum output voltage compliance is

\[
V_o (min) = V_P
\]

(9)

The schematic for the current source version of this circuit is shown in Figure 2 where a p-channel JFET is used.
IV. Cascode, Source-Biased JFET Current Sink/Source

While the output resistance of the single-stage current sink in Figure 1 can be reasonably large, another source-biased JFET current sink is capable of producing an output resistance that is several orders of magnitude greater. This is the cascode, source-biased JFET current sink shown in Figure 3. In this circuit, $J_1$ and $J_2$ are connected in the cascode configuration such that the output current $I_o$ is identical to the drain currents of both JFETs. To insure $J_1$ is operating in the saturation region, it is necessary that

$$V_{DS1} \geq V_{P1} \sqrt{\frac{I_o}{I_{DSS1}}}$$

(10)

To insure $J_2$ is operating similarly, $I_o$ is restricted by
Under these conditions, the output current is determined from the solution of a quadratic equation similar to that in equation (4); that is,

\[
I_o \leq \left( \frac{V_{p1}}{\sqrt{I_{DSS1}} + \sqrt{I_{DSS2}}} \right)^2
\]

(11)

where \(V_{p2}\) and \(I_{DSS2}\) are the pinch-off voltage and drain-source saturation current, respectively, of device \(J_2\). If these values are known, the source resistor \(R_S\) is determined from an equation similar to equation (5)

\[
R_S = \frac{V_{p2}}{I_o} \left( 1 - \frac{I_o}{\sqrt{I_{DSS2}}} \right)
\]

(13)

The small-signal output resistance \(R_o\) of the cascode sink is calculated from

\[
R_o = r_o + r_{o2} \left( 1 + g_m I_{o2} \right) + R_S \left[ 1 + g_{m2} r_{o2} \left( 1 + g_m I_{o2} \right) \right]
\]

(14)

which is much larger than \(R_o\) in equation (6) for the single-stage sink. The minimum output voltage compliance is determined from

\[
V_o (min) = V_{p1} + R_S I_o
\]

(15)

Clearly, the minimum compliance for the cascode design is greater than that for the single stage design. A cascode current source using PJFETs is shown in Figure 4.
V. JFET Model Parameter Extraction

Before the current sources and sinks in this experiment can be built, it is necessary to obtain the model parameters of the devices used in the circuits. Methods for extracting these parameters are explained in (2). For the two n-channel and two p-channel JFETs provided for this experiment, apply these methods to extract these parameters and list them in Table 1 below. Calculate $r_o$ at $I_D$ equal to 2mA.

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Type</th>
<th>$\lambda$ (V$^{-1}$)</th>
<th>$r_o$ (Ω)</th>
<th>$V_P$ (V)</th>
<th>$I_{DSS}$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>J111</td>
<td>NJFET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>J111</td>
<td>NJFET</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>J176</td>
<td>PJFET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>J176</td>
<td>PJFET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VI. NJFET Current Sink Measurements

Schematics for single-stage and cascode source-biased NJFET current sinks are shown in Figure 5. Design and build each of these circuits on your breadboard according to the output current specifications listed below. Take the necessary measurements listed below on each of these circuits.

(a) Set $V_{DD}$ to 10V and calculate the value of $R_S$ for a nominal value of $I_o$ of 2mA.
(b) Measure $R_S$ and record its value in Table 2.
(c) Measure $V_{DD}$ and $I_o$ for their nominal values; $V_{DD}(\text{nom})$ and $I_o(\text{nom})$. Record these values in Table 2.
(d) Vary $V_{DD}$ to measure values for the output resistance $R_o$ and the output regulation factor $S_3(I_o, V_{DD})$. Record these values in Table 2 for each current sink.
$$R_o = \frac{1}{\frac{\Delta I_o(V_{DD})}{\Delta V_{DD}}}$$

$$S_{so}(I_o, V_{DD}) = \frac{V_{DD}(nom)}{I_o(nom)} \frac{\Delta I_o(V_{DD})}{\Delta V_{DD}} = \frac{V_{DD}(nom)}{I_o(nom)} \frac{1}{R_o}$$  \hspace{1cm} (16)$$

(e) Set $V_{DD}$ to its nominal value and reduce it to measure the minimum compliance voltage $V_o\text{(min)}$. Record this value in Table 2 for each current sink.

Make use of these parameters in this table to determine which current sink performs the best.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Single-stage (Figure 5(a))</th>
<th>Cascode (Figure 5(b))</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_S$ (fixed) (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$ (nom) (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_o$ (nom) (A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_o$ (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$S_{3o}(I_o, V_{DD})$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_o$ (min)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VII. PJFET Current Source Measurements

Schematics for single-stage and cascode source-biased PJFET current sources are shown in Figure 6. Design and build each of these circuits on your breadboard according to the output current specifications listed below. Take the necessary measurements listed below on each of these circuits.

(a) Set $V_{DD}$ to 10V and calculate the value of $R_S$ for a nominal value of $I_o$ of 2mA.
(b) Measure $R_S$ and record its value in Table 3.
(c) Measure $V_{DD}$ and $I_o$ for their nominal values; $V_{DD}$(nom) and $I_o$(nom). Record these values in Table 3.
(d) Vary $V_{DD}$ to measure values for the output resistance $R_o$ and the output regulation factor $S_{3o}(I_o, V_{DD})$. Record these values in Table 3 for each current sink.

$$R_o = \frac{1}{\frac{\Delta I_o(V_{DD})}{\Delta V_{DD}}}$$

$$S_{so}(I_o, V_{DD}) = \frac{V_{DD}(nom)}{I_o(nom)} \frac{\Delta I_o(V_{DD})}{\Delta V_{DD}} = \frac{V_{DD}(nom)}{I_o(nom)} \frac{1}{R_o}$$  \hspace{1cm} (17)$$

(e) Set $V_{DD}$ to its nominal value and reduce it to measure the minimum compliance voltage $V_o\text{(min)}$. Record this value in Table 3 for each current sink.

Make use of these parameters in this table to determine which current sink performs the best.
Figure 6
(a) Single-stage source biased current source
(b) Cascode source biased current source

Table 3
Current source parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Single-stage (Figure 6(a))</th>
<th>Cascode (Figure 6(b))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rs (fixed) (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD(nom) (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Io(nom) (A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ro (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sth(Io,VDD)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vo(min)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VIII. References
I. Introduction
Junction field-effect transistors (JFET) make near ideal constant current sources and current sinks. This is due to the nearly constant drain current ($I_D$) that flows through the channel when the device is operating in a saturated condition. JFET saturation occurs when the drain end of the channel is closed or pinched off and the active channel volume does not change as the drain-source voltage ($V_{DS}$) is increased [1-4]. Since JFETs are depletion-mode devices, they can be self-biased with simple circuitry to produce current sources not requiring external power supplies. Self-biased JFET current sources are commonly known as current regulator diodes that find many applications in current regulation, current limiting, bias networks, and low voltage references, to name a few [5].

This note describes the large-signal dc model for the JFET and methods for extracting its parameters.

II. Large-Signal Device Model
The electronic symbols for silicon processed n-channel (NJFET) and p-channel (PJFET) JFETs are shown in Figure 1. In the saturation region, the gate-source voltage $V_{GS}$ is negative, the drain and source currents ($I_D$ and $I_S$) are equal, and the gate current $I_G$ is zero. The large-signal model for the NJFET that define the mathematical relationship between $I_D$, and $V_{GS}$ and $V_{DS}$ is given by the square-law equation

$$I_D = I_S = I_{DSS} \left[1 - \frac{(-V_{GS})}{V_P}\right]^2 (1 + \lambda V_{DS})$$  \hspace{1cm} (1)

The model parameters in this equation are the pinch-off voltage $V_P$ in volts, the drain-source saturation current $I_{DSS}$ in amperes, and the channel-length modulation parameter $\lambda$ in inverse volts (V$^{-1}$). For operation in the saturation region, $V_{GS}$ and $V_{DS}$ must satisfy the conditions

$$-V_P \leq V_{GS} \leq 0$$
$$V_{DS} \geq V_{DS} (sat) = V_P - (-V_{GS}) = V_P + V_{GS}$$  \hspace{1cm} (2)

![Figure 1](JFET electronic symbols)

2 The NJFET is used in the derivations and calculations that follow. Similar explanations and derivations can be performed for the PJFET where the polarities of current and voltages are reversed.
With $V_{DS}$ set to $V_{DS}(sat)$, the forward transfer characteristics are illustrated graphically with an IV plot of $I_D$ versus $V_{GS}$ generated from (1) where $V_{GS}$ controls $I_D$ with a square-law relationship. A typical forward transfer characteristics curve is shown in Figure 2. With $V_{GS}$ swept over a range from zero to a value greater than $-V_P$, the output characteristics of the device are also generated from (1) and shown graphically with the plot of $I_D$ versus $V_{DS}$. The family of curves resulting from several $V_{GS}$ values are shown in Figure 3 for a typical device. The separation of the curves in this graph are based on the square-law relationship described in (1). By extending the slope of the IV curve at $V_{GS} = 0$ with a straight line, the intersection of this line with the $V_{DS}$ axis yields the value of the inverse of $\lambda$. This is shown in Figure 3 where the slope of the straight line is the inverse of the small-signal output resistance $r_o$ of the device.

III. Parameter Extraction

These parameters are necessary in the design of many JFET circuits including current sources and can be extracted from dc measurements made on a typical device.

(a) Extraction of $\lambda$. The parameter $\lambda$ is extracted from the NJFET $\text{J}_{\text{DUT}}$ by biasing the device at $I_{DSS}$ with the gate shorted to the source for zero $V_{GS}$ as shown in Figure 4. With a known value for $R_D$, the drain load line is superimposed on the device output characteristics curve as shown in Figure 5. The slope $r_o$ is calculated from two points on the intersection of the output characteristics curve with the drain load line set by two values of the supply voltage $E_{DD}$ ($E_{DD1}$ and $E_{DD2}$) with

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{V_{DS2} - V_{DS1}}{I_{D2} - I_{D1}}$$

(3)

Using the equation of a triangle, an expression for $\lambda$ is derived from points on the extrapolated line for

$$\lambda = \frac{1}{r_o I_{D2} - V_{DS2}}$$

(4)

The expression for $r_o$ in (3) is inserted into (4) so that $\lambda$ is finally expressed as

$$\lambda = \frac{I_{D2} - I_{D1}}{V_{DS2}I_{D1} - V_{DS1}I_{D2}}$$

(5)

![Figure 2](image)

**Figure 2**

Typical NJFET forward transfer characteristics curve

---

3 ‘DUT’ is an acronym for ‘device under test’.
Figure 3
Typical NJFET output characteristics curves

Figure 4
NJFET biased at $I_{DSS}$

Figure 5
Output characteristic curve with drain load lines
while the expression for \( r_o \) in terms of \( \lambda \) is

\[
\frac{1 + \lambda V_{DS1}}{I_D} \]

(b) **Extraction of \( V_P \) and \( I_{DSS} \).** Once \( \lambda \) is known, \( V_P \) and \( I_{DSS} \) are extracted from the bias network shown in Figure 6 where a resistor \( R_S \) is placed in the source with the gate shorted to ground. The source voltage \( V_S \) is the voltage drop across \( R_S \) and is equal to the negative of the gate-source voltage for

\[
V_S = -V_{GS} = R_S I_D
\]

Inserting this expression for \( V_{GS} \) into (1), the drain current is written as

\[
I_D = I_{DSS} \left[ 1 - \frac{R_S I_D}{V_P} \right]^2 \left( 1 + \lambda V_{DS} \right)
\]

With two values of \( R_S \) inserted into (8), corresponding values for the drain current \( I_D \) are computed. These two values occur from the intersection of (7) and (8) as illustrated graphically on the JFET forward transfer characteristics curve in Figure 7. The expressions for these currents in terms of the source voltage \( V_S \) and the drain-source voltage \( V_{DS} \) are

\[
I_{D1} = I_{DSS} \left[ 1 - \frac{R_{S1} I_D}{V_P} \right]^2 \left( 1 + \lambda V_{DS1} \right) = I_{DSS} \left[ 1 - \frac{V_{S1}}{V_P} \right]^2 \left( 1 + \lambda V_{DS1} \right)
\]

\[
I_{D2} = I_{DSS} \left[ 1 - \frac{R_{S2} I_D}{V_P} \right]^2 \left( 1 + \lambda V_{DS2} \right) = I_{DSS} \left[ 1 - \frac{V_{S2}}{V_P} \right]^2 \left( 1 + \lambda V_{DS2} \right)
\]

Forming the ratio of \( I_{D1} \) to \( I_{D2} \) eliminates \( I_{DSS} \) resulting in a single expression for \( V_P \); that is,

\[
\frac{I_{D1}}{I_{D2}} = \left( \frac{V_P - V_{S1}}{V_P - V_{S2}} \right)^2 \left( \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}} \right)
\]

Solving for \( V_P \) gives

\[
V_P = \frac{V_{S1} - k V_{S2}}{1 - k}
\]

where the constant \( k \) is

\[
k = \sqrt{\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}} \frac{I_{D1}}{I_{D2}}
\]

Finally, \( I_{DSS} \) is computed from either of the expressions in (9) for

\[
I_{DSS} = \frac{I_{D1}}{\left( \frac{V_{S1}}{V_P} \right)^2 \left( 1 + \lambda V_{DS1} \right)} = \frac{I_{D2}}{\left( \frac{V_{S2}}{V_P} \right)^2 \left( 1 + \lambda V_{DS2} \right)}
\]
IV. Extraction Example

Parameters are extracted from a typical 2N3819 NJFET for the DUT. Measurements made on this device in the $\lambda$ extraction circuit shown in Figure 8 are listed in Table 1. Placing the data in this Table into (5), $\lambda$ is computed as

$$\lambda = \frac{I_{D2} - I_{D1}}{V_{DS2}I_{D2} - V_{DS1}I_{D2}} = \frac{6.892857mA - 6.852041mA}{(13.75 - 6.852041 - 8.70 - 6.892857)mA\cdot V}$$

$$\lambda = 1.191788 \cdot 10^{-3} V^{-1} = \frac{1}{839.0756V}$$

while $r_o$ at $V_{GS} = 0$ is computed from (6) for

$$r_o = \frac{1 + \lambda}{\lambda I_{D1}} = \frac{1 + 1.191788 \cdot 10^{-3} \cdot 8.70}{1.191788 \cdot 10^{-3} \cdot 6.852041 \cdot 10^{-3}} \Omega$$

$$r_o = 123.7260K\Omega$$

Next, the DUT is placed in the circuit shown in Figure 9 for the extraction of $V_P$ and $I_{DSS}$. With $E_{DD}$ set to 15V, voltage and current measurements are made with two values for $R_S$. These measurement are listed in Table 2 and used in (12) and (11) for the calculation of $k$ and $V_P$. For the constant $k$, (12) gives
\[ k = \sqrt{\frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}} \sqrt{\frac{I_{D1}}{I_{D2}}} = \sqrt{\frac{1 + 1.191788 \cdot 10^{-3} \cdot 13.31}{1 + 1.191788 \cdot 10^{-3} \cdot 13.56}} \frac{1.508032 mA}{0.9028777 mA} \]
\[ k = 1.292192 \]

which is inserted into (11) for \( V_P \) where

\[ V_P = \frac{V_{S1} - k V_{S2}}{1 - k} \]
\[ V_P = \frac{1.502 - 1.292192 \cdot 1.757}{1 - 1.292192} V \]
\[ V_P = 2.629713 V \] (17)

**Figure 8**
\( \lambda \) extraction circuit

<table>
<thead>
<tr>
<th>Point</th>
<th>( E_{DD} ) (V)</th>
<th>( V_{DS} ) (V)</th>
<th>( E_{DD} - V_{DS} ) (V)</th>
<th>( I_D ) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10.043</td>
<td>8.70</td>
<td>1.343</td>
<td>6.852041mA</td>
</tr>
<tr>
<td>2</td>
<td>15.101</td>
<td>13.75</td>
<td>1.351</td>
<td>6.892857mA</td>
</tr>
</tbody>
</table>

**Table 1**

Measurements for \( \lambda \) extraction, \( R_D = 196\Omega \)

**Figure 9**

\( V_P \) and \( I_{DSS} \) extraction circuit
Table 2
Measurements for $V_P$ and $I_{DSS}$ extraction, $E_{DD} = 10V$

<table>
<thead>
<tr>
<th>Point</th>
<th>$R_S$ (Ω)</th>
<th>$V_D = E_{DD}$ (V)</th>
<th>$V_S$ (V)</th>
<th>$V_{DS}$ (V)</th>
<th>$I_D = I_S$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>996</td>
<td>15.062</td>
<td>1.502</td>
<td>13.56</td>
<td>1.508032m</td>
</tr>
<tr>
<td>2</td>
<td>1.946K</td>
<td>15.067</td>
<td>1.757</td>
<td>13.31</td>
<td>0.9028777m</td>
</tr>
</tbody>
</table>

Finally, (13) is used to produce $I_{DSS}$ which is

$$I_{DSS} = \frac{I_D}{\left(1 + \frac{V_S}{V_P}\right)^2 (1 + \lambda V_{DS})} = \frac{1.508032mA}{\left(1 + \frac{1.502}{2.629713}\right)^2 \left(1 + 1.191788 \cdot 10^{-3} \cdot 13.56\right)}$$

(18)

$$I_{DSS} = 8.069891mA$$

In summary, the large-scale model parameters for the 2N3819 DUT are listed below

$$\lambda = 1.191788 \cdot 10^{-3} V^{-1} = \frac{1}{839.0756V}$$

$$r_o = 123.7260KΩ$$

$$V_P = 2.629713V$$

$$I_{DSS} = 8.069891mA$$

(19)

V. Conclusion

JFETs are important devices in the solid-state semiconductor library. They have been used extensively in many analog integrated circuit designs as well as discrete circuit designs. Significant applications in analog circuit designs include JFET differential amplifiers as front end stages in low-noise, high-speed operational amplifiers, pinch resistors used as start-up devices to initialize bias circuits, and, as mentioned in the Introduction, self-biased current sources known as current regulator diodes.

VI. References

VII. Appendix

Worksheet for the Extraction of JFET Model Parameters

1. *Large-signal JFET model:*

\[ I_D = I_S = I_{DSS} \left[ 1 - \frac{(-V_{GS})}{V_P} \right]^2 \left( 1 + \lambda V_{DS} \right) \]  

(1)

2. *Extraction of \( \lambda \) and \( r_o \):*

![Diagram](Figure 1)

(a) Bias circuit for extracting \( \lambda \) (\( R_D = \text{constant} \))

(b) \( J_DUT \) pin-out

![Diagram](Figure 1)

*Figure 1*

(a) Bias circuit for extracting \( \lambda \) (\( R_D = \text{constant} \))

(b) \( J_DUT \) pin-out

**Table 1**

| Measurements for \( V_{GS} = 0 \), \( R_D = \) ______Ω |
|---|---|---|---|---|
| Point | \( E_{DD} \) | \( V_D \) | \( E_{DD} - V_D \) | \( I_D \) |
| 1 | \( \) | \( \) | \( \) | \( \) |
| 2 | \( \) | \( \) | \( \) | \( \) |

(a) *Calculation of \( \lambda \) –*

\[
\lambda = \frac{I_{D2} - I_{D1}}{V_{D2}I_{D1} - V_{D1}I_{D2}}
\]

(2)

(b) *Calculation of \( r_o \) –*

\[
r_o = \frac{1 + \lambda V_{DS1}}{\lambda I_{D1}}
\]

(3)
3. Extraction of $V_P$ and $I_{DSS}$:

![Bias Circuit](image)

**Figure 2**
Bias circuit for extracting $V_P$ and $I_{DSS}$ ($E_{DD}$ = constant)

<table>
<thead>
<tr>
<th>Point</th>
<th>$R_S$</th>
<th>$V_D = E_{DD}$</th>
<th>$V_S$</th>
<th>$V_DS$</th>
<th>$I_D = I_S$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<tr>
<td>2</td>
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</tbody>
</table>

(a) Calculation of $V_P$ –

$$k = \sqrt{\frac{(1 + \lambda V_{DS1}) I_{D1}}{(1 + \lambda V_{DS2}) I_{D2}}} \quad (4)$$

$$V_P = \frac{V_{S1} - kV_{S2}}{1 - k} \quad (5)$$

(b) Calculation of $I_{DSS}$ –

$$I_{DSS} = \frac{I_{D1}}{\left(1 - \frac{V_{S1}}{V_P}\right)^2 \left(1 + \lambda V_{DS1}\right)} \quad (6)$$
Table 3
Extracted parameters

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Type</th>
<th>( \lambda ) (V(^{-1}))</th>
<th>( r_o ) (( \Omega ))</th>
<th>( V_P ) (V)</th>
<th>( I_{DSS} ) (A)</th>
</tr>
</thead>
<tbody>
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</table>
Lab Experiment No. 7

Biased Current Sinks and Sources

I. Introduction

The purpose of this lab is to evaluate the performance of biased dc constant currents sinks and sources. The circuits presented here represent a variety of commonly-used current sinks/sources built with BJTs and op-amps. The theory and equations associated with these circuits are covered in class lectures and Chapter 1 of your course notes. Your job in this session is to build, test and evaluate each of the given current sink/source circuits in order to expand your hands-on experience in working with these circuits. For each circuit, make use of the parts supplied by the GTA, and the DMM and dc power supply located on the lab bench.

II. Components and Instruments

The components and instruments required for this lab are listed below.

**Components:**
- Op-amp: TLC274
- NPN BJT: 2N3904 (4)
- PNP BJT: 2N3906 (4)
- Diode: 1N4148 (4)
- Capacitors: 220pF, 10uF
- Resistors: 330, 360, 1K, 7.5K, 8.2K, 9.1K, 20K

**Instruments:**
- Power supply
- Multimeter: Agilent E3620A, Agilent 34401A

**Additional:**
- Breadboard
- Tool box
- Hook-up wire

III. Characterization of Constant Current Sinks/Sources

Current sinks and sources are characterized with respect to their ability to maintain a constant output current in the presence of varying power supply voltages. Metrics for gauging this ability are provided by measuring the change in the output current with respect to changes in the supply voltage. The relative strength of these changes is formulated in terms of regulation factors known as line or input regulation and load or output regulation. In addition to these factors is the range of supply voltage for which the circuit can adequately operate. This is known as the voltage compliance range where the minimum value in this range is more important. The equivalent circuit of a simple constant current sink is shown in Figure 1(a) where the input and output stages are indicated. According to the voltage substitution theorem\(^4\), the power supply voltage \(V_{CC}\) is split into two voltage sources to bias the input and output stages separately. This is shown in Figure 1(b) where \(V_{CCi}\) and \(V_{CCo}\) are initially equal to \(V_{CC}\). The circuit model of the sink is shown in Figure 1(c) where the output current \(I_o\) is expressed as

\[
I_o(V_{CCi}, V_{CCo}) = I_c(V_{CC}) + \frac{V_{CCo}}{R_o}
\]

For an ideal current sink, \(I_c\) is completely independent of \(V_{CCi}\) and \(R_o\) has an infinite value. However, for a non-ideal sink, the current \(I_c(V_{CC})\) represents the component of \(I_o\) generated in the input stage and controlled by the supply voltage \(V_{CC}\) that biases this stage while the finite output resistance \(R_o\) represents the component of \(I_o\) controlled by the supply voltage \(V_{CCo}\). Changes in these voltages produce corresponding changes in \(I_o\) that can be measured independently. The

---

**input regulation** \( S_i(I_o, V_{CC}) \) is defined as the per-unit change in \( I_o \) caused by a per-unit change in \( V_{CC} \) with \( V_{CC_o} \) held constant at the nominal operating voltage of \( V_{CC} \); that is

\[
S_i(I_o, V_{CC}) = \frac{\Delta I_o(V_{CC}, V_{CC_o})}{I_o \frac{\Delta V_{CC}}{V_{CC}}} V_{CC_o} = V_{CC_o}(V_{CC_o} = V_{CC_{(nom)}})
\]

Based on the ratio of these changes, input regulation has no units although it has a magnitude and sign that measure the relative change in \( I_o \) with respect to \( V_{CC} \). The **output regulation** \( S_o(I_o, V_{CC}) \) is defined as the per-unit change in \( I_o \) caused by a per-unit change in \( V_{CC} \) with \( V_{CC_i} \) held constant at the nominal operating voltage of \( V_{CC} \); that is

\[
S_o(I_o, V_{CC}) = \frac{\Delta I_o(V_{CC}, V_{CC_o})}{I_o \frac{\Delta V_{CC}}{V_{CC}}} V_{CC_o} = V_{CC_o}(V_{CC_o} = V_{CC_{(nom)}})
\]

It is clear that output regulation also has no units and is measure of the relative change in \( I_o \) caused by a change in \( V_{CC_o} \). **Output resistance** \( R_o \) is also used to characterize the performance of a current sink. From Figure 1, \( R_o \) is defined as

\[
R_o = \frac{1}{\frac{\Delta I_o(V_{CC}, V_{CC_o})}{\Delta V_{CC_o}} V_{CC_o} = V_{CC_o}(V_{CC_o} = V_{CC_{(nom)}})}
\]
The last metric is the minimum value of the output voltage \(V_o(min)\) which defines the low end of the output compliance voltage. This voltage is the minimum value of \(V_{CCo}\) for which the transistor is not in deep saturation; that is,

\[
V_o(min) = V_{CCo}(min)
\]  

(5)

IV. Measurements

Photos of the breadboard layout of a typical current sink circuit are shown in Figures 2 and 3. The input and output stages of this sink are biased with separate supply voltages according to Figure 1(b). The supply voltages are labeled under the binding posts on the breadboard.

A. Input regulation

1. Set the power supply voltages \(V_{CCi}\) and \(V_{CCo}\) equal to the nominal voltage for \(V_{CC}(V_{CC}(\text{nom}))\). Measure the nominal value of the output current \(I_o(nom)\).
2. With \(V_{CCo}\) held constant, change \(V_{CCi}\) by \(\Delta V_{CCi}\) and measure \(I_o\); label as \(I_o(\Delta V_{CCi})\).
3. Calculate the input regulation \(S_3(I_o, V_{CCi})\) from

\[
S_3(I_o, V_{CCi}) = \frac{V_{CC}(nom)}{I_o(nom)} \left[ \frac{I_o(\Delta V_{CCi}) - I_o(nom)}{\Delta V_{CCi}} \right]
\]  

(6)

B. Output regulation

1. Set the power supply voltages \(V_{CCi}\) and \(V_{CCo}\) equal to the nominal voltage for \(V_{CC}(V_{CC}(\text{nom}))\). Measure the nominal value of the output current \(I_o(nom)\).
2. With \(V_{CCi}\) held constant, change \(V_{CCo}\) by \(\Delta V_{CCo}\) and measure \(I_o\); label as \(I_o(\Delta V_{CCo})\).
3. Calculate the output regulation \(S_3(I_o, V_{CCo})\) from

\[
S_3(I_o, V_{CCo}) = \frac{V_{CCo}(nom)}{I_o(nom)} \left[ \frac{I_o(\Delta V_{CCo}) - I_o(nom)}{\Delta V_{CCo}} \right]
\]  

(7)

C. Output resistance

1. Set the power supply voltages \(V_{CCi}\) and \(V_{CCo}\) equal to the nominal voltage for \(V_{CC}(V_{CC}(\text{nom}))\). Measure the nominal value of the output current \(I_o(nom)\).
2. With \(V_{CCi}\) held constant, change \(V_{CCo}\) by \(\Delta V_{CCo}\) and measure \(I_o\); label as \(I_o(\Delta V_{CCo})\).
3. Calculate the output resistance \(R_o(I_o, V_{CCo})\) from

\[
R_o(I_o, V_{CCo}) = \frac{1}{\frac{I_o(\Delta V_{CCo}) - I_o(nom)}{\Delta V_{CCo}}}
\]  

(8)

D. Minimum output compliance voltage

1. Set the power supply voltages \(V_{CCi}\) and \(V_{CCo}\) equal to the nominal voltage for \(V_{CC}(V_{CC}(\text{nom}))\). Measure the nominal value of the output current \(I_o(nom)\).
2. With \(V_{CCi}\) held constant, decrease \(V_{CCo}\) until the base-collector junction of the output transistor becomes forward biased.
3. Label \(V_o(min)\) with this value of \(V_{CCo}\).
Figure 2
Current sink breadboard layout

Figure 3
Current sink breadboard layout
V. DC Constant Current Sinks

A collection of three dc constant current sinks are shown in Figures 4 through 6. Design and build each of these circuits on your breadboard according to the bias and output current specifications listed below. Take the necessary measurements on each of these circuits to calculate the performance parameters listed in Table 1.

(a) \( I_{\text{bias}} = 1\, \text{mA}, I_o = 2\, \text{mA} \).
(b) With a nominal voltage for \( V_{CC} = 10\, \text{V} \), measure and record all node to ground voltages for a voltage and current map of each current sink circuit.
(c) Vary \( V_{CC} \) and \( V_{CC_o} \) to measure values for the input and output regulation factors, and the output resistance. Record these values in Table 1 for each current sink.
(d) Set \( V_{CC} \) to its nominal \( V_{CC} \) value and vary \( V_{CC_o} \) to measure the minimum compliance voltage \( V_o(\text{min}) \). Record this value in Table 1 for each current sink.

Make use of these parameters in this table to determine which current sink performs the best.

![Simple current sink with diode bias](image)

**Figure 4**
Simple current sink with diode bias

![Buffered current sink with diode bias](image)

**Figure 5**
Buffered current sink with diode bias
A collection of three dc constant current sources are shown in Figures 7 through 9. Design and build each of these circuits on your breadboard according to the bias and output current specifications listed below. Take the necessary measurements on each of these circuits to calculate the performance parameters listed in Table 2.

(a) $I_{\text{bias}} = 1\text{mA}$, $I_o = 2\text{mA}$.
(b) With a nominal voltage for $V_{\text{CC}} = 10\text{V}$, measure and record all node to ground voltages for a voltage and current map of each current source circuit.
(c) Vary $V_{\text{CC}}$ and $V_{\text{CCO}}$ to measure values for the input and output regulation factors, and the output resistance. Record these values in Table 2 for each current source.
(d) Set $V_{\text{CC}}$ to its nominal $V_{\text{CC}}$ value and vary $V_{\text{CCO}}$ to measure the minimum compliance voltage $V_o(\text{min})$. Record this value in Table 2 for each current source.

Make use of these parameters in this table to determine which current source performs the best.
Figure 7
Simple current source with diode bias

Figure 8
Buffered current source with diode bias
Figure 9
Current source with current-boosting transistor

Table 2
Current source parameters

<table>
<thead>
<tr>
<th>Figure</th>
<th>$S_3(I_o, V_{CCI})$</th>
<th>$S_3(I_o, V_{CCo})$</th>
<th>$R_o(I_o, V_{CCo})$ (Ω)</th>
<th>$V_o$(min) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>9</td>
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</tbody>
</table>

VII. Example
The schematic of the current sink shown in Figure 1(a) is shown below in Figure 10. This sink is biased with voltage sources $V_{CCI}$ and $V_{CCo}$ according to the circuit in Figure 1(b).

![Simple current sink with separate input and output bias](image)

(a) Design target:
$I_{bias} = 800µA$
$I_o = 2mA.$
Values shown for $R_1$ and $R_2$ are measured values.

(b) Measured values for a voltage and current map under nominal operating conditions:
$V_{CCI} = 10.089V$
$V_{CCo} = 10.0615V$
$V_{C1} = 4.2758V$
$V_{E1} = 3.6261V$
$V_{E2} = 3.6113V$
$V_{R1} = 5.8076V$
$I_{bias} = 779.3972µA$
$I_o = 2.0128mA$

(c) Measured values for regulation factors, output resistance and minimum output voltage compliance:
(i.) input regulation:

<table>
<thead>
<tr>
<th>Point</th>
<th>$V_{CCI}$ (V)</th>
<th>$I_o$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (nom)</td>
<td>10.0906</td>
<td>2.013m</td>
</tr>
</tbody>
</table>
\[ S_{3i} (I_o, V_{CCI}) = \frac{V_{CCI} (nom)}{l_o (nom)} \left[ \frac{\Delta I_o}{\Delta V_{CCI} \cdot V_{CCI}} \right] = \frac{V_{CCI}}{l_o}\left[ \frac{I_{o1} - I_{o2}}{V_{CCI} - V_{CCI2}} \cdot V_{CCI} \right] \]

\[ S_{3i} (I_o, V_{CCI}) = \frac{10.0906V}{2.013mA} \left[ \frac{2.013mA - 1.972mA}{10.0906V - 9.063V} \right] = 0.2 \tag{9} \]

(ii.) output regulation:

<table>
<thead>
<tr>
<th>Table 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurements for ( S_o(I_o, V_{CCI}) ) (( V_{CCI} = 10.0901V ))</td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td><strong>Point</strong></td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td>1 (nom)</td>
</tr>
<tr>
<td>2</td>
</tr>
</tbody>
</table>

\[ S_{3o} (I_o, V_{CCI}) = \frac{V_{CCI} (nom)}{l_o (nom)} \left[ \frac{\Delta I_o}{\Delta V_{CCI} \cdot V_{CCI}} \right] = \frac{V_{CCI}}{l_o}\left[ \frac{I_{o1} - I_{o2}}{V_{CCI} - V_{CCI2}} \cdot V_{CCI} \right] \]

\[ S_{3o} (I_o, V_{CCI}) = \frac{10.067V}{2.013mA} \left[ \frac{2.013mA - 2.0123mA}{10.067V - 9.0418V} \right] = 0.003413 \tag{10} \]

(iii.) output resistance

\[ R_{o} (I_o, V_{CCI}) = \frac{1}{\Delta I_o} = \frac{1}{\Delta V_{CCI}} \cdot \frac{I_{o1} - I_{o2}}{V_{CCI} - V_{CCI2}} = \frac{1}{\Delta I_o} \cdot \frac{I_{o1} - I_{o2}}{V_{CCI} - V_{CCI2}} = \frac{1}{\Delta I_o} \cdot \frac{2.013mA - 2.0123mA}{10.067V - 9.0418V} = 1.465143 \Omega \tag{11} \]

(iv.) minimum compliance voltage:

\( V_{CCI} = 10.0704V \)
\( V_{CCI} = 4.3933V \)
\( V_{CB2} \approx 0V \)
\( V_o(min) = 4.3933V \)
Lab Experiment No. 8  

**Current Mirrors**

I. **Introduction**
The purpose of this lab exercise is to investigate the operation and performance of transistor current mirrors. The circuits presented here represent a variety of commonly-used current mirrors built with NPN and PNP BJTs. The theory and equations associated with these circuits are covered in class lectures and Chapter 1 of your course notes. Your job in this session is to design, build, and test each current mirror to expand your hands-on experience in working with these circuits. Make use of the parts supplied by the GTA and the instruments located on the lab bench to perform this investigation.

II. **Components and Instruments**
The components and instruments required for this lab are listed below.

**Components:**
- Resistors: 160Ω 330Ω (2) 620Ω 10KΩ

**Transistors –**
- NPN: 2N3904 (8)
- PNP: 2N3906 (8)
- NJFET: J113
- PJFET: J176

**Instruments:**
- Power supply  Agilent E3620A
- Multimeter  Agilent 34401A
- Additional: Breadboard  Tool box  Hook-up wire

III. **Characterization of Current Mirrors**
Current mirrors play important roles in a wide variety of analog circuits both discrete and integrated. These subcircuits are instrumental in transferring and scaling bias and signal currents around the host circuit for the realization of precise high-speed responses. Due to design similarities, current mirrors share common characteristics with current sinks and sources. Output resistance $R_o$ and minimum compliance voltage $V_{oc}(\text{min})$ are two important parameters associated with mirrors. Precise current scaling and sensitivity to load changes are also important mirror parameters.
IV. NPN Current Mirror Topologies
Schematics for three multiple output NPN current mirrors are shown in Figure 1 through 3. These mirrors are the buffered Widlar, the cascode, and the four transistor Wilson. The reference current \( I_{\text{ref}} \) supplied to each of these mirrors is 2mA while the outputs are scaled replicas of \( I_{\text{ref}} \) ranging from 1mA to 4mA as indicated. The circuit shown in Figure 4 is a current source that provides \( I_{\text{ref}} \) to these mirrors. Your job is to do the following.

(a) Design each mirror to replicate (mirror) the 2mA input reference \( I_{\text{ref}} \) into the unloaded output currents \( I_{oa} \), \( I_{ob} \), and \( I_{oc} \) of 4mA, 2mA, and 1mA, respectively. Generate \( I_{\text{ref}} \) from the single-stage, source-biased PIFET current source built in Lab 2(b). You will have to design this circuit as well.

(b) Test the performance of each mirror by measuring the output currents \( (I_{oa}, I_{ob}, \text{and } I_{oc}) \), the output resistance of each output \( (R_{oa}, R_{ob}, \text{and } R_{oc}) \) and the minimum compliance voltage of each output \( (V_{oa}(\text{min}), V_{ob}(\text{min}), \text{and } V_{oc}(\text{min})) \). Enter these values into Table 1 where indicated.

(c) Draw schematics for all circuits (mirrors and current sources) complete with component values.
NPN cascode current mirror

Figure 3
NPN Wilson current mirror

Figure 4
I_{ref} source for an NPN current mirror
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Buffered Widlar</th>
<th>Cascode</th>
<th>Wilson</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ref}$</td>
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<tr>
<td>$I_{oa}$</td>
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<td>$I_{ob}$</td>
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<td>$I_{oc}$</td>
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<td>$R_{oa}$</td>
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<td>$R_{ob}$</td>
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<td>$R_{oc}$</td>
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<td>$V_{oa}(\text{min})$</td>
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<td>$V_{ob}(\text{min})$</td>
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<td>$V_{oc}(\text{min})$</td>
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</table>
V. PNP Current Mirror Topologies

Schematics for three multiple output PNP current mirrors are shown in Figure 5 through 7. These mirrors are the buffered Widlar, the cascode, and the four transistor Wilson. The reference current \( I_{\text{ref}} \) supplied to each of these mirrors is 2mA while the outputs are scaled replicas of \( I_{\text{ref}} \) ranging from 1mA to 4mA as indicated. The circuit shown in Figure 8 is a current sink that provides \( I_{\text{ref}} \) to these mirrors. Your job is to do the following.

(a) Design each mirror to replicate (mirror) the 2mA input reference \( I_{\text{ref}} \) into the unloaded output currents \( I_{oa}, I_{ob}, \) and \( I_{oc} \) of 4mA, 2mA, and 1mA, respectively. Generate \( I_{\text{ref}} \) from the single-stage, source-biased NJFET current sink built in Lab 2(b). You will have to design this circuit as well.

(b) Test the performance of each mirror by measuring the output currents (\( I_{oa}, I_{ob}, \) and \( I_{oc} \)), the output resistance of each output (\( R_{oa}, R_{ob}, \) and \( R_{oc} \)) and the minimum compliance voltage of each output (\( V_{oa}(\text{min}), V_{ob}(\text{min}), \) and \( V_{oc}(\text{min}) \)). Enter these values into Table 2 where indicated.

(c) Draw schematics for all circuits (mirrors and current sources) complete with component values.

![Figure 5](image1)

**Figure 5**
PNP buffered Widlar current mirror

![Figure 6](image2)

**Figure 6**
PNP cascode current mirror
Figure 7
PNP Wilson current mirror

Figure 8
I_{ref} circuit for a PNP current mirror
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Buffered Widlar</th>
<th>Cascode</th>
<th>Wilson</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ref}$</td>
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<td>$I_{oa}$</td>
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<td>$V_{oc}(\text{min})$</td>
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</table>
Lab Experiment No. 9

BJT Bias Networks

I. Introduction
Bipolar junction transistors (BJT) must be properly biased in the forward operating region (aka, the linear active region) to perform effectively in analog signal processing networks such as amplifiers. The circuits studied in this lab experiment are two of those typically employed in the electronics industry to bias single-stage NPN and PNP BJTs. The theory and equations associated with these circuits are covered in class lectures and your course notes. Your job in this experiment consists of three components –
(a) design – apply your analytical skills to design the bias network that will meet a given set of specifications,
(b) simulate – simulate your design with PSPICE to verify its performance, and
(c) fabrication – build your design on a breadboard and take measurements to further verify actual performance.
In addition to calculating resistor values to set the dc bias point, sensitivity functions are also computed and applied in generating a bias figure of merit (FOM). The FOM is used to compare the bias stability of these two circuits.

II. Components and Instruments
The components and instruments required for this experiment are listed below.

Components:
- BJT:
  - NPN BJT 2N3904
  - PNP BJT 2N3906

Instruments:
- Power supply
- Multimeter
  - Agilent E3620A
  - Agilent 34401A
- Function generator
- Oscilloscope
  - Agilent 33120A
  - Tektronics MDO3052

Additional:
- Breadboard
- Tool box
- Hook-up wire
- Assorted resistors (to be determined)

III. Application and Measurement of $S_3$ Sensitivity Functions
$S_3$ sensitivity functions can be applied to produce a metric to gauge the stability of a bias circuit. As discussed in class lectures, these functions are generated from the ratio of the per unit change in the quiescent collector current to the per unit change in a circuit variable such as a resistor or a device parameter. For example, with all resistors set to their nominal values in Figure 1, if a change in resistor $R_{B1}$ ($\Delta R_{B1}$) produces a corresponding change in $I_{CQ}$ ($\Delta I_{CQ}$), the $S_3$ sensitivity function of $I_{CQ}$ with respect to $R_{B1}$ is calculated from

$$ S_3\left(I_{CQ}, R_{B1}\right) = \frac{\Delta I_{CQ}}{I_{CQ}(nom)} = \frac{R_{B1}(nom) \Delta I_{CQ}}{\Delta R_{B1} \frac{I_{CQ}(nom)}{R_{B1}(nom)}} $$

where $R_{B1}(nom)$ and $I_{CQ}(nom)$ are the nominal values of the base bias resistor $R_{B1}$ and the quiescent collector current $I_{CQ}$, respectively. Based on equation (1), $S_3$ functions establish a clear indication of how sensitive the collector current is to bias circuit components and parameters. For example, if the magnitude of $S_3$ is greater than one, the circuit is somewhat sensitive to $R_{B1}$ while if $S_3$’s magnitude is less than one, the circuit is not so sensitive to the resistor. It is obvious the terms ‘somewhat’ and ‘not so’ are dependent on the actual value of the magnitude. Considering the calculated resistor values of the bias circuit to be independent variables, the figure of merit (FOM) $F_3$ is generated from the sum of the absolute values of resistor $S_3$ functions; that is

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where ‘x’ denotes the bias resistor subscript (B1 for RB1, B2 for RB2, etc.). For a bias circuit designed to be insensitive to its bias resistors and therefore highly stable, it is necessary that it have a very small F3. Therefore, this FOM can be used to compare bias circuits for their relative stability. The circuit with the smaller F3 is the more stable. The circuits shown in Figures 2(a) and 2(b) can be used to measure the variables necessary to calculate the S3 functions with the following operations –

(i) connect in series with each bias resistor a resistor (referred to as the ‘Δ resistor’) that is approximately 1% to 5% of the nominal bias resistor value; for example, if RB1 is 100KΩ, connect a Δ resistor (ΔRB1) of 1KΩ in series with RB1,
(ii) short all Δ resistors with wire jumpers as shown in Figure 2(a) for the nominal circuit,
(iii) measure the quiescent collector current for ICQ(nom),
(iv) remove the wire jumper from the Δ resistors one at a time (shown in Figure 2(b)) and measure the new value of the collector current ICQ(new), this current is the value of ICQ produced by the effect of the Δ resistor (ΔRx) on the corresponding bias resistor (Rx),
(v) calculate the sensitivity function S3(ICQ, Rx) from

\[ S_3 \left( I_{CQ}, R_x \right) \equiv \frac{R_x}{I_{CQ}^{(nom)}} \frac{I_{CQ}^{(new)} - I_{CQ}^{(nom)}}{\Delta R_x} \]  

(vi) repeat the above for all resistors.

These functions are used to calculate F3 from equation (2).

IV. Voltage Divider Bias Circuit

The NPN BJT 2N3904 and the PNP BJT 2N3906 are biased with the voltage divider circuits shown in Figures 3(a) and 3(b), respectively. Branch currents and node voltages are indicated on the schematic for each network. Model parameters for Q1 are given below –

\[ \beta_F = 100 \]
\[ V_{BE} = V_{EB} = 0.675V @ 1.0mA \]
\[ I_{CBO} = 0 \]
The transistors biased in these circuits are to meet the following specifications –

\[
\begin{align*}
V_{CC} &= 15\text{V} & \text{dc supply voltage} \\
I_{CQ} &= \frac{I_C (\text{max})}{2} = 1.0\text{mA} & \text{dc collector current} \\
R_{in} &= \frac{1}{\beta F + 1}R_E = 14\text{K}\Omega & \text{base input resistance} \\
S_3(I_{CQ}, \beta F) &= 0.2 & \text{sensitivity of } I_{CQ} \text{ with respect to } \beta F
\end{align*}
\]  

(a) **Design** – Use the model parameters in equation (4) to calculate values for resistors \(R_{B1}, R_{B2}, R_E, \text{ and } R_C\) that will bias \(Q_1\) to realize the specifications listed in equation (5) for the circuits in Figure 3(a) and 3(b). Use these resistors to calculate values for the node voltages, branch currents, and the circuit dissipated power \(P_{\text{diss}}\). The power dissipated by the circuit is computed from the product of the power supply voltage and current; that is,

\[
P_{\text{diss}} = V_{CC}I_{CC}
\]  

List resistor values in the top part of Table 1(a) for the NPN circuit of Figure 3(a) and the top part of Table 2(a) the PNP circuit of Figure 3(b) under the column labeled ‘Design’, and the currents, voltages, and \(P_{\text{diss}}\) in the bottom part of the table where indicated for a voltage and current map of the circuit. Use these resistor values and BJT model parameters to calculate the \(S_3\) functions with respect to bias resistors \((R_{B1}, R_{B2}, R_E, \text{ and } R_C)\) and transistor beta \((\beta F)\). Place these \(S_3\) values in the first column of Table 1(b) and Table 2(b). Use these functions to calculate the sums at the bottom of the table column.

(b) **Simulation** – Replace all resistors with standard values as close as possible to the calculated values. Simulate the resulting circuit with the PSPICE circuit simulator. If necessary, vary the values of \(R_{B1}\) and/or \(R_{B2}\) to adjust the dc collector current \(I_{CQ}\) of 1.0mA within ±5\% \((950\mu\text{A} \leq I_{CQ} \leq 1.05\text{mA})\). List the resistor values in the top part of Table 1(a) and Table 2(a) under the column labeled ‘Simulation’, and the currents, voltages, and \(P_{\text{diss}}\) in the bottom part of...
the Table where indicated for a voltage and current map of the circuit. Perform circuit simulations necessary to generate the $S_I$ functions with respect to bias resistors ($R_{B1}, R_{B2}, R_E,$ and $R_C$) and transistor beta ($\beta_F$). Place these $S_I$ values in the second column of Table 1(b) and Table 2(b). Use these functions to calculate the sums at the bottom of the Table column.

(c) Fabrication – Build the bias circuit on your breadboard with standard resistor values determined in part (b). Provide a hand-drawn schematic of your design with all component values. Again, if necessary, vary the values of $R_{B1}$ and/or $R_{B2}$ to adjust the dc collector current $I_{CQ}$ to be within ±5% of the 1.0mA specification. List all resistor values in the top part of Table 1(a) and Table 2(a) under the column labeled ‘Fabrication’. Measure and record all dc node voltages, branch currents, and $P_{diss}$ in the bottom part of the Table where indicated. Change resistor values and measure the resulting voltages and currents necessary to calculate the $S_I$ functions from your fabricated bias circuit shown in Figure 2(a) and 2(b). Place these $S_I$ values in the third column of Table 1(b) and Table 2(b). Use these functions to calculate the sums at the bottom of the Table column.
### Table 1(b)
NPN voltage divider bias sensitivity functions

<table>
<thead>
<tr>
<th>Component (x_i)</th>
<th>( S_3(I_{CQ}, x_i) ) (design)</th>
<th>( S_3(I_{CQ}, x_i) ) (simulation)</th>
<th>( S_3(I_{CQ}, x_i) ) (fabrication)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{B1} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{B2} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_E )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \beta_F )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Sigma S_3(I_{CQ}, x_i) )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( F_3 = \Sigma</td>
<td>S_3(I_{CQ}, x_i)</td>
<td>)</td>
<td></td>
</tr>
</tbody>
</table>

### Table 2(a)
PNP voltage divider bias network

<table>
<thead>
<tr>
<th>Component</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{B1} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{B2} )</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( R_E )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>15V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{CQ} )</td>
<td>1.0mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_B )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_E )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 102 -
\[
\begin{array}{|c|c|}
\hline
V_{EB} (V_E - V_R) & 0.65V \\
I_B & \\
\beta_F (I_{CQ}/I_B) & 100 \\
I_E & \\
I_{RB1} & \\
I_{RB2} & \\
I_{CC} & \\
P_{diss} & \\
\hline
\end{array}
\]

**Table 2(b)**

PNP voltage divider bias sensitivity functions

<table>
<thead>
<tr>
<th>Component ((x_i))</th>
<th>(S_3(I_{CQ}, x_i)) (design)</th>
<th>(S_3(I_{CQ}, x_i)) (simulation)</th>
<th>(S_3(I_{CQ}, x_i)) (fabrication)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{B1})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{B2})</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>(R_E)</td>
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<td></td>
<td></td>
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<tr>
<td>(R_C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\beta_F)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Sigma S_3(I_{CQ}, x_i))</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(F_3 = \Sigma</td>
<td>S_3(I_{CQ}, x_i)</td>
<td>)</td>
<td></td>
</tr>
</tbody>
</table>

V. Self-Bias Circuit

The second circuit studied in this experiment is the collector feedback circuit known also as the self-bias circuit. The schematic for this circuit is shown in Figure 4(a) which is used to bias the NPN BJT 2N3904 and Figure 4(b) to bias the PNP BJT 2N3906. As for the previous circuit, branch currents and node voltages are shown on the circuit. Model parameters for \(Q_1\) are given below.

\[
\beta_F = 100 \\
V_{BE} = V_{EB} = 0.675V @ 1.0mA \\
I_{CBO} = 0
\]

(7)

These circuits are to be designed to meet the following specifications –

\[
V_{CC} = 15V \quad \text{dc supply voltage} \\
I_{CQ} = 1.0mA \quad \text{dc collector current} \\
S_3(I_{CQ}, \beta_F) = 0.3 \quad \text{sensitivity of } I_{CQ} \text{ with respect to } \beta_F \\
\frac{R_C}{R_E} = 6 \quad \text{R}_C \text{ to } R_E \text{ ratio}
\]

(8)
(a) **Design** – Use the model parameters in equation (7) to calculate values for resistors $R_B$, $R_E$, and $R_C$ that will bias $Q_1$ to realize the specifications listed in equation (8) for the circuits shown in Figures 4(a) and 4(b). Use these resistors to calculate values for the node voltages, branch currents, and the circuit dissipated power $P_{\text{diss}}$. List resistor values in the top part of Table 3(a) for the NPN circuit of Figure 4(a) and the top part of Table 4(a) the PNP circuit of Figure 4(b) under the column labeled ‘Design’, and the currents, voltages, and $P_{\text{diss}}$ in the bottom part of the table where indicated for a voltage and current map of the circuit. Use these resistor values and BJT model parameters to calculate the $S_3$ functions with respect to bias resistors ($R_B$, $R_E$, and $R_C$) and transistor beta ($\beta_F$). Place these $S_3$ values in the first column of Table 3(b) and Table 4(b).

(b) **Simulation** – Replace all resistors with standard values as close as possible to the calculated values. Simulate the resulting circuit with the PSPICE circuit simulator. If necessary, vary the value of $R_B$ to adjust the dc collector current $I_{CQ}$ of 1.0mA within ±5% (950µA ≤ $I_{CQ}$ ≤ 1.05mA). List the resistor values in the top part of Table 3(a) and Table 4(a) under the column labeled ‘Simulation’, and the currents, voltages, and $P_{\text{diss}}$ in the bottom part of the Table where indicated for a voltage and current map of the circuit. Perform circuit simulations necessary to generate the $S_3$ functions with respect to bias resistors ($R_B$, $R_E$, and $R_C$) and transistor beta ($\beta_F$). Place these $S_3$ values in the second column of Table 3(b) and Table 4(b). Use these functions to calculate the sums at the bottom of the Table column.

(c) **Fabrication** – Build the bias circuit on your breadboard with standard resistor values determined in part (b). Provide a hand-drawn schematic of your design with all component values. Again, if necessary, vary the value of $R_B$ to adjust the dc collector current $I_{CQ}$ to be within ±5% of the 1.0mA specification. List all resistor values in the top part of Table 3(a) and Table 4(a) under the column labeled ‘Fabrication’. Measure and record all dc node voltages, branch currents, and $P_{\text{diss}}$ in the bottom part of the Table where indicated. Change resistor values and measure the resulting voltages and currents necessary to calculate the $S_3$ functions from your fabricated bias circuits similar to those shown in Figure 2(a) and 2(b). Place these $S_3$ values in the third column of Table 3(b) and Table 4(b). Use these functions to calculate the sums at the bottom of the Table column.
<table>
<thead>
<tr>
<th>Component</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_B$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_E$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_C$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Variable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CQ}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_C$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_B$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_E$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BE}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
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<tr>
<td>$\beta_F$</td>
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<tr>
<td>$I_E$</td>
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<td></td>
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</tr>
<tr>
<td>$I_{EE}$</td>
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<tr>
<td>$P_{diss}$</td>
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</table>

<table>
<thead>
<tr>
<th>Component $(x_i)$</th>
<th>$S_3(I_{CQ}, x_i)$ (design)</th>
<th>$S_3(I_{CQ}, x_i)$ (simulation)</th>
<th>$S_3(I_{CQ}, x_i)$ (fabrication)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_B$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_E$</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$R_C$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\beta_F$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Sigma S_3(I_{CQ}, x_i)$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$F_3 = \Sigma</td>
<td>S_3(I_{CQ}, x_i)</td>
<td>$</td>
<td></td>
</tr>
<tr>
<td>Component</td>
<td>Design</td>
<td>Simulation</td>
<td>Fabrication</td>
</tr>
<tr>
<td>-----------</td>
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<td>------------</td>
<td>-------------</td>
</tr>
<tr>
<td>(R_B)</td>
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<td></td>
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<tr>
<td>(R_E)</td>
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<td></td>
<td></td>
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<tr>
<td>(R_C)</td>
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<tr>
<td>Variable</td>
<td>Design</td>
<td>Simulation</td>
<td>Fabrication</td>
</tr>
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<td></td>
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<tr>
<td>(I_{CQ})</td>
<td>1.0mA</td>
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<td></td>
</tr>
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<td>(V_C)</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>(V_B)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_E)</td>
<td></td>
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</tr>
<tr>
<td>(V_{EB}) ((V_E - V_R))</td>
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<tr>
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</tr>
<tr>
<td>(\beta_F(I_{CQ}/I_B))</td>
<td>100</td>
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<td></td>
<td></td>
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<tr>
<td>(I_{EE})</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>(P_{diss})</td>
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<td></td>
</tr>
</tbody>
</table>

### Table 4(b)

<table>
<thead>
<tr>
<th>Component ((x_i))</th>
<th>(S_3(I_{CQ}, x_i)) ((\text{design}))</th>
<th>(S_3(I_{CQ}, x_i)) ((\text{simulation}))</th>
<th>(S_3(I_{CQ}, x_i)) ((\text{fabrication}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_B)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_E)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_C)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>(\beta_F)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>(\Sigma S_3(I_{CQ}, x_i))</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(F_3 = \Sigma</td>
<td>S_3(I_{CQ}, x_i)</td>
<td>)</td>
<td></td>
</tr>
</tbody>
</table>

#### VI. Comparisons

Apply the data in the above Tables to compare these designs to each other with respect to the following:

(a) the accuracy of the design equations presented in lectures for calculating resistor values to fabricate the specified collector current \(I_{CQ}\) of 1.0mA,

(b) the amount of resistor adjustment in \% necessary to fabricate the specified collector current \(I_{CQ}\) of 1.0mA,

(c) the circuit that has the smallest value for \(F_3\), and

(d) the circuit that provides the largest degree of bias stability.

Include these topics of comparison in your lab report.
Lab Experiment No. 10

MOSFET Bias Networks

I. Introduction
Enhancement mode MOSFETs must be biased in the saturation region where the drain-source voltage \(V_{DS}\) is greater than drain-source saturation voltage \(V_{DS(sat)}\). This will allow the device to perform effectively in analog signal processing networks such as amplifiers. The circuits studied in this lab experiment are two bias networks typically employed in the electronics industry to bias single-stage n-channel and p-channel MOSFETs. The theory and equations associated with these circuits are covered in class lectures and your course notes. Your job in this experiment consists of three components –
(a) design – apply your analytical skills to design the bias network that will meet a given set of specifications,
(b) simulate – simulate your design with PSPICE to verify its performance, and
(c) fabrication – build your design on a breadboard and take measurements to further verify actual performance.

II. Components and Instruments
The components and instruments required for this experiment are listed below.
Components:
MOSFETs:
  n and p-channel ALD1103
JFETs:
  NJFET J111
  PJFET J175
Resistors:
  470Ω  680Ω  1KΩ  1.2KΩ  47KΩ  68KΩ
  Others determined by students.

Instruments:
  Power supply
  Agilent E3620A
  Multimeter
  Agilent 34401A
  Function generator
  Agilent 33120A
  Oscilloscope
  Tektronics MDO3052
  Additional:
  Breadboard
  Tool box
  Hook-up wire

III. NMOS Voltage Divider Bias Network
One of the simplest bias networks for an n-channel MOSFET is the voltage divider network shown in Figure 1. This network uses four resistors and a single dc voltage source to bias the n-channel device \(M_1\) at a given dc operating point.

With values specified for the quiescent drain current \(I_{DQ}\), the input resistance at the gate (\(R_{in}\)), and the source resistance \(R_s\), the following equations are used to calculate the other resistances in the network

\[
\begin{align*}
R_s + R_p &= 0.5 \left( \frac{V_{DD}}{I_{DQ}} + \frac{1}{\sqrt{\beta I_{DQ}}} \right) \\
R_{G1} &= \frac{V_{DD} R_s}{\sqrt{\frac{I_{DQ}}{\beta} + V_{TH} + R_s I_{DQ}}} \\
R_{G2} &= \frac{1}{\frac{1}{R_{in}} - \frac{1}{R_{G1}}} 
\end{align*}
\]

(1)
where the battery voltage \( V_{DD} \) and the MOSFET model parameters \( \beta \) and \( V_{TH} \) are given.

(a) **Design** – The NMOS device to be biased with the voltage divider network is device M1 on the ALD1103 integrated circuit (IC) chip. DC bias specifications and device model parameters are given below.

\[
\begin{align*}
V_{DD} &= 9V \\
I_{DQ} &= 1.25mA \\
R_{in} &= 400K\Omega \\
R_S &= 680\Omega \\
\beta &= 1.051mA/V^2 \\
V_{TH} &= 0.4728V
\end{align*}
\]  

Apply equation (1) to calculate values for resistors \( R_D \), \( R_{G1} \), and \( R_{G2} \) that will bias M1 to realize these specifications for the circuit in Figure 1. Use these resistors to calculate values for the node voltages, branch currents, and the circuit dissipated power \( P_{diss} \). The power dissipated by the circuit is computed from the product of the power supply voltage and current; that is,

\[
P_{diss} = V_{DD}I_{DD}
\]  

List resistor values in the top part of Table 1 under the column labeled ‘Design’, and the currents, voltages, and \( P_{diss} \) in the bottom part of the Table where indicated for a voltage and current map of the circuit.

(b) **Simulation** – Replace all resistors with standard values as close as possible to the calculated values. Simulate the resulting circuit with the PSPICE circuit simulator. PSPICE model parameters for the ALD1103 devices are listed in the Appendix to this experiment. If necessary, vary the values of \( R_{G1} \) and/or \( R_{G2} \) to adjust the quiescent drain current \( I_{DQ} \) of 1.25mA within \( \pm 5\% \) \( (1.1875mA \leq I_{DQ} \leq 1.3125mA) \). List the resistor values in the top part of Table 1 under the column labeled ‘Simulation’, and the currents, voltages, and \( P_{diss} \) in the bottom part of the Table where indicated for a voltage and current map of the circuit.

(c) **Fabrication** – Build the bias circuit on your breadboard with standard resistor values determined in part (b). Provide a hand-drawn schematic of your design with all component values. Again, if necessary, vary the values of \( R_{G1} \) and/or \( R_{G2} \) to adjust \( I_{DQ} \) to be within \( \pm 5\% \) of the 1.25mA specification. List all resistor values in the top part of Ta-
ble 1 under the column labeled ‘Fabrication’. Measure and record all dc node voltages, branch currents, and $P_{\text{diss}}$ in the bottom part of the Table where indicated.

<table>
<thead>
<tr>
<th>Component</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{G1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{G2}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_D$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_S$</td>
<td>680Ω</td>
<td>680Ω</td>
<td>680Ω</td>
</tr>
<tr>
<td>Variable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>9V</td>
<td>9V</td>
<td></td>
</tr>
<tr>
<td>$V_G$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_D$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DQ}$</td>
<td>1.25mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{G1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{G2}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{in}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{\text{diss}}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 1**

NMOS voltage divider bias network

IV. PMOS Voltage Divider Bias Network

The voltage divider bias network for an enhancement mode PMOS device is shown in Figure 2. Equations for the resistors are identical to those in equation (1). Use these equations to design a PMOS bias network that will meet the following specifications.

\[
V_{DD} = 15V\quad \text{dc supply voltage}
\]
\[
I_{DQ} = 2.5mA\quad \text{quiescent drain current}
\]
\[
R_{in} = 500K\Omega\quad \text{gate input resistance}
\]
\[
R_S = 470\Omega\quad \text{source resistance}
\]
\[
\beta = 1.051mA/V^2\quad \text{PMOS transconductance parameter}
\]
\[
V_{TH} = 0.4728V\quad \text{PMOS threshold voltage}
\]

Repeat the design, simulation, and fabrication process previously used on an NMOS device to the design of a voltage divider network shown in Figure 2 for a PMOS device. Apply these components in your design procedure to fill out Table 2.
$M_1 = \text{PMOS from ALD1103}$

**Figure 2**
PMOS voltage divider bias network

### Table 2
PMOS voltage divider bias network

<table>
<thead>
<tr>
<th>Component</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{G1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{G2}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_D$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_S$</td>
<td>$470\Omega$</td>
<td>$470\Omega$</td>
<td>$470\Omega$</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>15V</td>
<td>15V</td>
<td></td>
</tr>
<tr>
<td>$V_G$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_D$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DQ}$</td>
<td>2.5mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{G1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{G2}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{in}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{diss}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
V. NMOS Current Source Bias Network

A more direct way to bias a MOSFET at a specified drain voltage and current is to force a constant current into its drain terminal. A network that will provide a constant bias current to an NMOS device is shown in Figure 3. N-channel JFET J1 and resistor Rs1 form a self-biased current sink that sets the reference current I_{ref}. PMOSFETs M1 and M2 are connected as a current mirror to mirror I_{ref} into I_{bias}. If M1 and M2 are identical devices, then I_{bias} = I_{ref}. Assuming that IF is much smaller than I_{bias}, M1’s quiescent drain current I_{D3Q} is approximately equal to I_{bias} and I_{ref}. Under these conditions, the quiescent drain voltage V_{D3Q} is determined from the gate voltage V_{G3} with

\[ V_{D3Q} = \left(1 + \frac{R_F}{R_{G3}}\right)V_{G3} \]

(5)

where V_{G3} is calculated from M1’s bias voltages which are functions of its drain current.

(a) Design – The NMOS device to be biased with the current source bias network is device M1 on the ALD1103 integrated circuit (IC) chip. DC bias specifications and device model parameters are given below.

\[
\begin{align*}
V_{DD} &= 10V \\
I_{D3Q} &= 2.0mA \\
V_{D3Q} &= 4.5V \\
R_{G3} &= 47K\Omega \\
R_{S3} &= 1K\Omega \\
\beta &= 1.051mA/V^2 \\
V_{TH} &= 0.4728V
\end{align*}
\]

Design this network by calculating values for resistors Rs1 and Rf3 that will bias M1 to realize these specifications for the circuit in Figure 3. Use these resistors to calculate values for the currents I_{ref}, I_{bias}, and I_{D3Q}, and the node voltages V_{G3}, V_{D3Q}, and V_{S3}. List resistor values in the top part of Table 3 under the column labeled ‘Design’, and the currents and voltages in the bottom part of the Table where indicated for a voltage and current map of the circuit.

(b) Simulation – Replace all resistors with standard values as close as possible to the calculated values. Simulate the resulting circuit with the PSPICE circuit simulator. PSPICE model parameters for J1 and the ALD1103 devices are listed in the Appendix to this experiment. If necessary, vary the values of Rs1 and/or Rf3 to adjust the quiescent drain current I_{D3Q} at 2.0mA within ±5% (2.1mA ≤ I_{D3Q} ≤ 1.9mA) and the quiescent drain voltage V_{D3Q} at 4.5V within ±5% (4.725V ≤ V_{D3Q} ≤ 4.275V). List the resistor values in the top part of Table 3 under the column labeled ‘Simulation’, and the currents and voltages in the bottom part of the Table where indicated for a voltage and current map of the circuit.

(c) Fabrication – Build the bias circuit on your breadboard with standard resistor values determined in part (b). Provide a hand-drawn schematic of your design with all component values. Again, if necessary, vary the values of Rs1 and/or Rf3 to adjust I_{D3Q} to be within ±5% of the 2.0mA specification and V_{D3Q} to be within ±5% of the 4.5V specification. List all resistor values in the top part of Table 3 under the column labeled ‘Fabrication’. Measure and record all node voltages and branch currents in the bottom part of the Table where indicated.
**Figure 3**
Constant current bias network for an NMOS device

**Table 3**
NMOS current source bias network

<table>
<thead>
<tr>
<th>Component</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{S1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{F3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{G3}$</td>
<td>47KΩ</td>
<td>47KΩ</td>
<td>47KΩ</td>
</tr>
<tr>
<td>$R_{S3}$</td>
<td>1KΩ</td>
<td>1KΩ</td>
<td>1KΩ</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable</th>
<th>Design</th>
<th>Simulation</th>
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</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>10V</td>
<td>10V</td>
<td></td>
</tr>
<tr>
<td>$V_{G3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{D3Q}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{S3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ref}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{D3Q}$</td>
<td>2.0mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_F$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
VI. PMOS Current Source Bias Network

The current source bias network for an enhancement mode PMOS device is shown in Figure 4. Design a PMOS bias network that will meet the following specifications.

\[
\begin{align*}
V_{DD} &= 12\text{V} & \text{dc supply voltage} \\
I_{D3Q} &= 2.0\text{mA} & \text{quiescent drain current} \\
V_{D3Q} &= 5.5\text{V} & \text{quiescent drain voltage} \\
R_{G3} &= 68\text{K}\Omega & \text{gate resistance} \\
R_{S3} &= 1.2\text{K}\Omega & \text{source resistance} \\
\beta &= 1.051\text{mA/V}^2 & \text{NMOS transconductance parameter} \\
V_{TH} &= 0.4728\text{V} & \text{NMOS threshold voltage}
\end{align*}
\]

Repeat the design, simulation, and fabrication process previously used on an NMOS device to the design of a voltage divider network shown in Figure 2 for a PMOS device. Apply these components in your design procedure to fill out Table 2.

![Figure 4](image_url)

Figure 4

Constant current bias network for a PMOS device
### Table 4
PMOS current source bias network

<table>
<thead>
<tr>
<th>Component</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{S1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{F3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{G3}$</td>
<td>68KΩ</td>
<td>68KΩ</td>
<td>68KΩ</td>
</tr>
<tr>
<td>$R_{S3}$</td>
<td>1.2KΩ</td>
<td>1.2KΩ</td>
<td>1.2KΩ</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable</th>
<th>Design</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>12V</td>
<td>12V</td>
<td></td>
</tr>
<tr>
<td>$V_{G3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DQ}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{S3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ref}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DQ}$</td>
<td>2.0mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_F$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VII. Comparisons**

Apply the data in the above Tables to compare these designs to each other with respect to the following:

(a) the accuracy of the design equations presented in lectures for calculating resistor values to fabricate the specified quiescent drain currents,
(b) the amount of resistor adjustment in % necessary to fabricate the specified drain currents, and
(c) the network for NMOS and PMOS bias that provides the largest degree of bias stability.

Include these topics of comparison in your lab report.

**VIII. Appendix: Device PSPICE Models**

*PSPICE model for the ALD1103 NMOS device (August 7, 2015)*

```plaintext
.model MALD03N NMOS
+(LEVEL=3
  L=10E-6
+W=880E-6
+TOX=6.0E-8
+WD=4.0E-7
+VTO=0.73
+RS=0.74
+DELTA=2.5
+XJ=1.3E-6
+ETA=0.913
+NFS=3.0E11
+CGDO=5.99E-10
+PB=0.90
+CGDO=5.99E-10
+VQ=0.4)
```
*PSPICE model for the ALD1103 PMOS device (August 7, 2015)
.model MALD03P PMOS
+(LEVEL=3          L=10E-6
+W=880E-6          TPG=1
+TOX=6.0E-8        LD=2.08E-6
+WD=4.0E-7         U0=550
+VTO=-0.73         THETA=0.222
+RS=0.74           RD=0.74
+DELTA=2.5         NSUB=1.57E16
+XJ=1.3E-6         VMAX=4.38E6
+ETA=0.913         KAPPA=0.074
+NFS=3.0E11        CGSO=5.99E-10
+CGDO=5.99E-10     CGBO=4.31E-10
+PB=0.90           XQC=0.4)

*PSPICE model for the J111 NJFET device (August 19, 2015)
.model J111 NJF
+(Beta=2.91m       Betatce=-.5
+Rd=1              Rs=1
+Lambda=17.5m      Vto=-4.047
+Vtotc=-2.5m       Is=205.2f
+Isr=1.988p        N=1
+Nr=2              Xti=3
+Alpha=20.98u      Vk=123.7
+Cgd=6.46p         M=.4069
+Pb=1              Fc=.5
+Cgs=5.74p         Kf=37.86E-18
+Af=1)

*PSPICE model for the J175 PJFET device (August 19, 2015)
.model J175 PJF
+(Beta=1.031m      Betatce=-.5
+Rd=1              Rs=1
+Lambda=28m        Vto=-3.762
+Vtotc=-2.5m       Is=461.5f
+Isr=4.402p        N=1
+Nr=2              Xti=3
+Alpha=32.54u      Vk=393.2
+Cgd=6.5p          M=.2789
+Pb=1              Fc=.5
+Cgs=9p            Kf=66.61E-18
+Af=1)
I. Introduction
The purpose of this lab exercise is to design single-stage BJT amplifiers. The circuits presented here are single-stage BJT class-A amplifiers biased with preferred biasing methods. The theory and equations associated with these circuits are covered in class lectures and course notes. Your job in this session is to design, build, and test each amplifier to expand your hands-on experience in working with these circuits. Make use of the parts supplied by the GTA and the instruments located on the lab bench to produce these amplifiers.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
Resistors:
200Ω  470Ω  620Ω  1KΩ  1.3KΩ  1.6KΩ  4.7KΩ  10KΩ  39KΩ  270KΩ  300KΩ  680KΩ  750KΩ
BJTs:
NPN BJT:  2N3904
PNP BJT:  2N3906
Capacitors:
10uF (2)  50uF
Potentiometer:
1KΩ trim pot

Instruments:
Power supply  Multimeter
Agilent E3620A  Agilent 34401A
Function generator  Oscilloscopes
Agilent 33120A  Agilent 54621A and MDO3052

Additional:
Breadboard
Tool box
Hook-up wire

III. Voltage Divider Bias Amplifier Circuit
A single-stage NPN amplifier biased by the voltage divider circuit is shown in Figure 1. The amplifier is driven by a transducer consisting of the ac small-signal source $V_S(s)$ and the 200Ω source resistance $R_S$. The load driven by the amplifier is the 10KΩ load resistor $R_L$. 
Definitions

\[
A_{\text{vt}}(s) = \frac{V_v(s)}{V_{\text{in}}(s)} \mid_{R_e=0, \quad R_l=\infty} \quad \text{unloaded terminal voltage gain}
\]

\[
A_{\text{vt}}(s) = \frac{V_v(s)}{V_S(s)} \mid_{R_e=200\Omega, \quad R_l=10K\Omega} \quad \text{loaded transducer voltage gain}
\]

\[
Z_{\text{in}}(s) = \text{input impedance with } R_1 \text{ connected}
\]

\[
Z_{\text{out}}(s) = \text{output impedance with } R_S \text{ connected}
\]

Device model parameters

Model parameters for Q1:

\[
\beta_F = 150
\]

\[
V_{\text{BE}} = 0.65V \ @ \ 500\mu A
\]

\[
I_{CBO} = 0
\]

Amplifier specifications

Design this amplifier to meet the following specifications:

\[
V_{\text{CC}} = 10V \quad \text{dc supply voltage}
\]

\[
I_{CQ} = \frac{I_{\text{CQ(max)}}}{2} = 500\mu A \quad \text{dc collector current}
\]

\[
Z_{\text{in}}(0) = \frac{R_{BB}}{1/(\beta+1)R_E1} = 75K\Omega \quad \text{input impedance at dc}
\]

\[
S_3\left(I_{CQ}, \beta_F\right) = 0.3 \quad \text{sensitivity of } I_{CQ} \text{ with respect to } \beta_F
\]

\[
\left|A_{\text{vt}} (3KHz)\right| = \frac{V_v}{V_{\text{in}}} \mid_{R_e=0, \quad R_l=\infty, \quad f=3KHz} = 10.0V/V \quad \text{unloaded terminal voltage gain at 3KHz}
\]

(a) Trim the values of \(R_{B1}\) and/or \(R_{B2}\) to obtain a dc collector current \(I_{CQ}\) of 500\(\mu A\) within \(\pm 5\% \ (475\mu A \leq I_{CQ} \leq 525\mu A)\).

(b) To adjust the magnitude of the terminal voltage gain \(A_{\text{vt}}\) at 3KHz, apply the emitter circuit shown in Figure 2 where \(R_{Ep}\) is a 1K\(\Omega\) trim pot.

Measurements

(a) Provide a hand-drawn schematic of your design with all component values.

(b) Measure and record all dc node voltages and branch currents in the voltage and current map Table 1(a).

(c) Measure and record in Table 1(b) the indicated amplifier parameters. Include drawn schematics illustrating how these parameters are measured.
Figure 1
Voltage divider bias circuit

Figure 2
Adjustable emitter circuit

Table 1(a)
Measured voltage and current map

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_C$</td>
<td></td>
</tr>
<tr>
<td>$V_B$</td>
<td></td>
</tr>
<tr>
<td>$V_E$</td>
<td></td>
</tr>
<tr>
<td>$I_{RB1}$</td>
<td></td>
</tr>
<tr>
<td>$I_{RB2}$</td>
<td></td>
</tr>
<tr>
<td>$I_{CQ}$</td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td></td>
</tr>
<tr>
<td>$I_E$</td>
<td></td>
</tr>
</tbody>
</table>
Table 1(b)
Amplifier parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>1KHz</th>
<th>3KHz</th>
<th>10KHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>(</td>
<td>A_v(\omega)</td>
<td>)</td>
<td></td>
</tr>
<tr>
<td>(</td>
<td>A_{vs}(\omega)</td>
<td>)</td>
<td></td>
</tr>
<tr>
<td>(</td>
<td>Z_{in}(\omega)</td>
<td>)</td>
<td></td>
</tr>
<tr>
<td>(</td>
<td>Z_{out}(\omega)</td>
<td>)</td>
<td></td>
</tr>
</tbody>
</table>

IV. Self-Bias Amplifier Circuit
A single-stage amplifier that employs a PNP BJT biased in the self-bias circuit is shown in Figure 3. This amplifier is driven by a transducer similar to the one in Figure 1 and also drives a 10KΩ load resistor \(R_L\). Definitions of the various voltage gains and driving-point impedance functions are identical to those for the previous amplifier.

Device model parameters
Model parameters for \(Q_1\):

\[
\beta_F = 150 \\
v_{BE} = 0.65V \text{ at } 1.5mA \\
I_{CBO} = 0
\]

Amplifier specifications
Design this amplifier to meet the following specifications:

\[
V_{CC} = 15V \\
I_{CQ} = 1.5mA \quad \text{dc supply voltage} \\
I_{CQ} = 1.5mA \quad \text{dc collector current} \\
S_3(I_{CQ}, R_F) = -0.2 \quad \text{sensitivity of } I_{CQ} \text{ with respect to } R_F \\
\frac{R_C}{R_E} = 6 \quad \text{R}_C \text{ to } R_E \text{ ratio} \\
\left|A_v(3KHz)\right| = \frac{V_o}{V_{in}} \bigg|_{R_f=0} = 10.0V/V \quad \text{unloaded terminal voltage gain at 3KHz}
\]

(a) Trim the value of \(R_B\) to obtain a dc collector current \(I_{CQ}\) of 1.5mA within ±5% (1.425mA ≤ \(I_{CQ} \leq 1.575mA\)).
(b) To adjust the magnitude of the terminal voltage gain \(A_v\) at 3KHz, apply the emitter circuit shown in Figure 2 where \(R_E\) is a 1KΩ trim pot.

Measurements
(a) Provide a hand-drawn schematic of your design with all component values.
(b) Measure and record all dc node voltages, branch currents, and the sensitivity of \(I_{CQ}\) with respect to \(R_B\) \((S_3(I_{CQ}, R_B))\) in the voltage and current map Table 2(a).
(c) Measure and record in Table 2(b) the indicated amplifier parameters. Include drawn schematics illustrating how these parameters are measured.
$V_S(s)$

$R_S$

$200\,\Omega$

$C_i$

$C_E$

$R_{E1}$

$R_{E2}$

$+V_{CC}$

$V_{E}$

$V_C$

$Q_1$

$V_B$

$I_CQ$

$V_{out}(s)$

$Z_{out}(s)$

$Z_{in}(s)$

$V_{in}(s)$

$V_{o}(s)$

$C_0$

$50\mu F$

$10\mu F$

$10\mu F$

$10K\Omega$

$V_B$

$V_C$

$V_E$

$I_{RB}$

$I_{RC}$

$I_{CQ}$

$I_B$

$I_E$

$S_3(I_{CQ}, R_B)$

Figure 3

Self-bias circuit

Table 2(a)

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_C$</td>
<td></td>
</tr>
<tr>
<td>$V_B$</td>
<td></td>
</tr>
<tr>
<td>$V_E$</td>
<td></td>
</tr>
<tr>
<td>$I_{RB}$</td>
<td></td>
</tr>
<tr>
<td>$I_{RC}$</td>
<td></td>
</tr>
<tr>
<td>$I_{CQ}$</td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td></td>
</tr>
<tr>
<td>$I_E$</td>
<td></td>
</tr>
<tr>
<td>$S_3(I_{CQ}, R_B)$</td>
<td></td>
</tr>
</tbody>
</table>

$Q_1 = MPS8598$ PNP
<table>
<thead>
<tr>
<th>Parameter</th>
<th>1KHz</th>
<th>3KHz</th>
<th>10KHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>A_v(\omega)</td>
<td>$</td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>A_m(\omega)</td>
<td>$</td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>Z_{in}(\omega)</td>
<td>$</td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>Z_{out}(\omega)</td>
<td>$</td>
<td></td>
</tr>
</tbody>
</table>

V. Lab Report
(a) Provide detailed schematics of your designs. Explain in detail your methods for measuring small-signal voltage gain, and input and output impedance. Provide schematics for these methods and label all equipment used. Explain any difficulties encountered with these methods.
(b) Compare the gain and impedance results of the two amplifier topologies and comment on which one is the better of the two in terms of calibration and measurement.
Lab Experiment No. 12

Operational Amplifier Design

I. Introduction
The purpose of this lab exercise is to build and test an operational amplifier (op-amp). The op-amp presented here is a voltage feedback type constructed from discrete PJFET (J271), NPNBJT (2N3904), and PNPBJT (2N3906). Your job in this session is to build and test the given circuit to expand your hands-on experience in working with op-amps. Make use of the parts supplied by the GTA and the instruments located on the lab bench to perform this experiment.

II. The OP3444b op-amp
The schematic and symbol for the OP3444b BJT voltage feedback operational amplifier (VFOA) is shown in Figure 1(a) and (b), respectively. The nominal operating conditions for this amplifier are given below.

\[
\begin{align*}
V_{CC} &= V_{EE} = 5.0V \\
T &= 27^\circ C
\end{align*}
\]

In this lab session, you will become familiar with important procedures and steps involved in the actual design cycle of an op-amp such as this one.

Part 1. Design. Calculate the value of the resistor \(R_{bias}\) in the source of \(J_1\) that will set the amplifier bias current (\(I_{bias}\)) to 2mA. Assume \(J_1\) has the model parameters listed below.

\[
\begin{align*}
I_{DSS} &= 10mA \\
V_p &= V_{GS(off)} = 2.5V \\
\lambda &= 0
\end{align*}
\]

You may assume the op-amp is nearly ideal so that when placed in this test circuit the input voltages (\(V_{p}\) and \(V_{n}\)), and the output voltage and current (\(V_{out}\) and \(I_{out}\)) are zero. Use these conditions to calculate the complete dc voltage and current map of the op-amp in the open-loop configuration. Record these voltages and currents in the first column of Table 1.

Part 2. Analytical. With \(I_{bias}\) of 2mA, perform a first-order pencil and paper circuit analysis of the op-amp in the open-loop test circuit shown in Figure 2. Use the transistor parameters below for this analysis.

\[
\begin{align*}
\beta &= \infty \text{ (for all transistors except } Q_7 \text{ and } Q_8) \\
\beta_7 &= \beta_b = 100 \\
V_{BE} &= 0.65V
\end{align*}
\]

You may assume the op-amp is nearly ideal so that when placed in this test circuit the input voltages (\(V_{p}\) and \(V_{n}\)), and the output voltage and current (\(V_{out}\) and \(I_{out}\)) are zero. Use these conditions to calculate the complete dc voltage and current map of the op-amp in the open-loop configuration. Record these voltages and currents in the first column of Table 1.

Part 3. Simulation. Simulate the OP3444b with PSPICE. Use the SPICE Gummel-Poon (SGP) model for the 2N3904 (NPN) and 2N3906 (PNP) BJTs, and the Shichman-Hodges model for the J271 PJFET provided in the PSPICE library.

(a) Place a battery (\(V_{id}\)) across the differential input terminals as shown in Figure 3. Adjust \(R_{bias}\) to set \(I_{bias}\) to 2mA. Record the value of \(R_{bias}\) in the second column of Table 1 where indicated.

(b) Sweep the voltage \(V_{id}\) to generate and plot the open-loop output voltage transfer curve (VTC). From the VTC, calculate the input offset voltage (\(V_{os}\)) and the differential mode voltage gain (\(G_{\Delta in}\)).

(c) In the circuit in Figure 3, set \(V_{id}\) equal to \(V_{os}\) in order to set \(V_{out}\) to zero; that is \(V_{id} = V_{os}\) so that \(V_{out} = 0V\). Perform a dc operating point simulation on the amplifier to obtain the open-loop dc voltages and currents shown on the schematic in Figure 1(a). Record these voltages and currents in the second column of Table 1.

Part 4. Breadboard. Build the OP3444b on a breadboard with J271, 2N3904, and 2N3906 transistors, 1% discrete resistors, and 5% capacitors.

(a) Bias the breadboard op-amp with the closed-loop circuit shown in Figure 4(a). Adjust \(R_{bias}\) to set \(I_{bias}\) to 2mA. Record the value of \(R_{bias}\) in the third column of Table 1 where indicated.
Figure 1
(a) OP3444b schematic
(b) Symbol
(b) Measure the complete dc voltage and current map. Record these voltages and currents in the third column of Table 1.

(b) Place the op-amp in the inverting-gain configuration in Figure 4(b)
   (1) generate the Bode plot of the closed-loop voltage gain magnitude (dB), and
   (2) record values for the closed-loop parameters in Table 2.

Part 5. Compare and comment.
(a) Compare the values of $R_{\text{bias}}$ and the dc voltages and currents recorded in Table 1. Comment on the accuracy of analytical calculations versus simulation versus actual breadboard measurements. How close are the values from calculations and simulations to the actual measured values?
(b) Comment on the inverting gain amplifier performance results recorded in Table 2.
(c) Comment on any major differences among the data in the tables. Determine reasons for these differences.

![Figure 2](image1.png)
Open-loop test circuit for pencil and paper analysis

![Figure 3](image2.png)
Open-loop test circuit for simulation of the VTC
**Figure 4**
(a) Closed-loop zero input test circuit for dc measurements
(b) Inverting gain amplifier configuration

**Table 1**
DC Voltage and Current Map

<table>
<thead>
<tr>
<th>Voltage/current</th>
<th>Analytical</th>
<th>Simulation</th>
<th>Breadboard</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{bias} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{EE} )</td>
<td>5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{S1} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{B2} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{E1} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{E2} )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 125 -
<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{E3}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{E4}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{E5}$</td>
<td></td>
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</tr>
<tr>
<td>$V_{E13}$</td>
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<tr>
<td>$V_{E18}$</td>
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<td></td>
</tr>
<tr>
<td>$V_p$</td>
<td>0.0V</td>
<td></td>
</tr>
<tr>
<td>$V_n$</td>
<td>0.0V</td>
<td></td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>0.0V</td>
<td></td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{C2}$</td>
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</tr>
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</tr>
<tr>
<td>$I_{C12}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td>Breadboard</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>$G_{Vd}(0)$</td>
<td>DC voltage gain</td>
<td></td>
</tr>
<tr>
<td>$f_{AI}$</td>
<td>-3dB Bandwidth</td>
<td></td>
</tr>
<tr>
<td>GBW$_i$</td>
<td>Gain-bandwidth product</td>
<td></td>
</tr>
<tr>
<td>SR$_p$</td>
<td>Positive slope slew-rate</td>
<td></td>
</tr>
<tr>
<td>SR$_n$</td>
<td>Negative slope slew-rate</td>
<td></td>
</tr>
</tbody>
</table>

**Table 2**

Inverting gain amplifier performance
Lab Experiment No. 13

Amplifier Networks

I. Introduction
The purpose of this lab session is to gain familiarity with several well-known amplifier circuits built with standard operational amplifiers. The theory and derivations associated with each of the circuits listed below has been covered both in class and in homework assignments. Basically, your job in this session is to design (where necessary), build, test, and evaluate each of these circuits in order to expand your hands-on experience in working with operational amplifiers. For each circuit listed below, use TLC274 operational amplifiers, standard 5% resistors, a ±5 volt dc power supply, and an ac signal generator. For measurements, use ac voltmeters, DVMs, and oscilloscopes.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:

<table>
<thead>
<tr>
<th>Resistor Values</th>
<th>Capacitor Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>510Ω</td>
<td>10nF</td>
</tr>
<tr>
<td>5.1KΩ</td>
<td>6.8μF</td>
</tr>
<tr>
<td>10KΩ</td>
<td>others as needed</td>
</tr>
<tr>
<td>18KΩ</td>
<td></td>
</tr>
<tr>
<td>20KΩ</td>
<td></td>
</tr>
<tr>
<td>30KΩ</td>
<td></td>
</tr>
<tr>
<td>39KΩ</td>
<td></td>
</tr>
<tr>
<td>51KΩ</td>
<td></td>
</tr>
</tbody>
</table>

Op-Amp: TLC-274

Instruments:

Function generator
Agilent 33120A 15MHz

Power supply
Agilent E3620A

Oscilloscope
Agilent 54621A 60MHz dual-channel
Agilent 34401A

Additional:

Breadboard
Tool box
Hook-up wire
Oscilloscope probes

III. Lab Assignment
Build and perform measurements on the following amplifier networks. Use dual ±5V power supply voltages for amplifier designs 1 through 4 (described in A through D below) and a single +10V power supply voltage for amplifier designs 5 and 6 (described in E and F below).

A. Amplifier No. 1. An inverting gain amplifier with a dc voltage gain of -5.0V/V and an input resistance of 10.0KΩ. Measure and plot the magnitude of the voltage gain (dB) over frequency from 10Hz to 15MHz. Indicate on this plot the -3dB bandwidth and calculate the amplifier GBW.

B. Amplifier No. 2. A non-inverting gain amplifier with a dc voltage gain of +4.0V/V and an input resistance of 10.0KΩ. Measure and plot the magnitude of the voltage gain (dB) over frequency from 10Hz to 15MHz. Indicate on this plot the -3dB bandwidth and calculate the amplifier GBW.

C. Amplifier No. 3. A dual-input difference amplifier with a dc voltage gain of ±2.0V/V and input resistances of 10.0KΩ. Measure and plot the magnitude of the voltage gain (dB) for each input over frequency from 10Hz to 15MHz. Indicate on this plot the -3dB bandwidth and calculate the GBW for each input.

D. Amplifier No. 4. The bridge amplifier (see problem 1.74 Ref. 1, Ref. 2) shown in Figure 1. Design this amplifier for a differential output voltage gain of +8V/V. Determine the maximum undistorted peak-to-peak voltage swing across the load resistor R_L at 1KHz.

E. Amplifier No. 5. The single supply non-inverting gain amplifier shown in Figure 2. Design this amplifier for a dc voltage gain of +6.5V/V, an input resistance (R_in) of 25KΩ, and balanced op-amp input terminals. Measure and plot the magnitude of the voltage gain (dB) over frequency from 10Hz to 15MHz. Indicate on this plot the -3dB bandwidth and calculate the amplifier GBW.

F. Amplifier No. 6. The single supply inverting gain amplifier shown in Figure 3. Design this amplifier for a dc voltage gain of -4.75V/V, an input resistance (R_in) of 37KΩ, and balanced input op-amp input terminals. Measure and plot the magnitude of the voltage gain (dB) over frequency from 10Hz to 15MHz. Indicate on this plot the -3dB bandwidth and calculate the amplifier GBW.
IV. References

V. Figures

![Bridge amplifier diagram](image1.png)

**Figure 1**
Bridge amplifier
(aka Boomer Amplifier)

![Single supply non-inverting gain amplifier diagram](image2.png)

**Figure 2**
Single supply non-inverting gain amplifier
Figure 3
Single supply inverting gain amplifier
Lab Experiment No. 14  
Op-Amp Test and Measurement

I. Introduction
The purpose of this lab exercise is to test an operational amplifier (op-amp) and to measure a set of its open-loop parameters. The results of these measurements provide important parameters for an op-amp data sheet. Your job in this lab experiment is to apply test circuit OATC1 shown in Figure 1 to a given device under test (DUT). The description of this test circuit and the procedures for taking measurements from the DUT are explained in the paper "OATC1: A Universal Test Circuit for Measuring Op-Amp Parameters" attached to this experiment. Make use of the parts and the DUT supplied by the GTA, and the instruments located on the lab bench to perform this experiment.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
- Op-amp: OP-07 (3)  LM741 DUT
- Capacitors: 300nF, NPO multilayer ceramic
- Resistors:
  - 100Ω (2)
  - 2KΩ (5)
  - 30KΩ
  - 51KΩ (3)
  - 100KΩ (2)
- Potentiometer: 10K, trimpot

Instruments:
- Power supply: Agilent E3620A
- Multimeter: Agilent 34401A
- Function generator: Agilent 33120A
- Oscilloscope: Agilent 54621A

Additional:
- Breadboard
- Tool box
- Hook-up wire

III. Op-amp Parameters and the Data Sheet
Download the data sheet for the LM741 op-amp. From this data sheet, extract the parameters listed in Table 1. Fill out the first column in Table 1 with these parameters. Build test circuit OATC1 on your breadboard with the LM741 connected as the device under test (DUT). Apply the procedures outlined in the attached paper to measure the parameters listed in Table 1. Fill out the second column of Table 1 with these measured values.

IV. Compare and Comment
(a) Compare the parameter values listed in Table 1. How close are the LM741 data sheet parameters to those from actual measurements? How useful is the test circuit OATC1 for generating a data sheet for an op-amp?
(b) Comment on any major differences among the data in Table 1. Determine reasons for these differences.

V. References

VI. Attachments
Figure 1
Op-amp test circuit OATC1

Table 1
DUT parameters
\((V_{psp}/V_{psn} = 10V, R_L = 2K\Omega, T = 27^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>LM741 Data sheet</th>
<th>OATC1</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{os})</td>
<td>Input offset voltage</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input bias current</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>(I_{BOS})</td>
<td>Input bias offset current</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>(P_{diss})</td>
<td>Power dissipation</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>PSRR(_p)</td>
<td>Positive power supply rejection ratio</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>PSRR(_n)</td>
<td>Negative power supply rejection ratio</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(G_{vdm}(0))</td>
<td>Open-loop dc differential-mode voltage gain</td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>(G_{vcm}(0))</td>
<td>Open-loop dc common-mode voltage gain</td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
</tbody>
</table>
OATC1: A Universal Test Circuit for Measuring Op-Amp Parameters

The circuit shown in Figure 1(a) is the test circuit OATC1 for the measurement of a variety of operational amplifier parameters. This circuit is an adaptation of the one shown on Intersil Corporation’s application note AN551.1 entitled “Recommended Test Procedures for Operational Amplifiers”. You may download this note from the company web site www.intersil.com. A similar circuit may be found in problem 5.27 on pages 246-247 of Sergio Franco’s textbook5.

![Circuit Diagram](image)

**Figure 1**
(a) OATC1 op-amp test circuit
(b) dc voltage generator

The $V_{psp}$ and $V_{psn}$ dc voltage rails are nominal power supply voltages required to bias the device under test (DUT) while $V_{id}$ and $V_{ic}$ represent differential-mode and common-mode input voltages to the DUT. These voltages are obtained from the circuit shown in Figure 1(b) which generates a low-impedance dc voltage set by $R_p$. Resistor values shown on the schematic are typical with 1% tolerances and can be changed if necessary. Assuming that the OP07s in this circuit are ideal op-amps, routine circuit analysis produces the following low-frequency, small-signal expression for the output voltage $V_{o2}$.

\[ V_{id} = \left( \frac{R_6}{R_s} \right) \left( \frac{R_3}{R_3 + R_7} \right) G_{vdm} (V_{o2} - V_{ic}) - \left( \frac{R_6}{R_s} \right) G_{vcm} V_{ic} + \left( \frac{R_6}{R_s} \right) G_{vdm} (V_{os} + R_p I_p - R_n I_n) \]  

(1)

where

\[ R_p = R_1 + R_2 \]

\[ R_n = R_4 + \frac{R_1 R_7}{R_3 + R_7} \]  

(2)

These equations are used in the procedures that follow to measure a series of low-frequency op-amp parameters. In these procedures, the indicated changes in \( V_{id} \) and \( V_{ic} \) are provided by the dc voltage generator with ± values.

1. **Input offset voltage** \( V_{os} \)
   a. close switches \( S_2 \) and \( S_4 \),
   b. set \( V_{ic} \) and \( V_{id} \) to zero by connecting pins 1 and 2 to ground,
   c. measure \( V_{o2} \) with a dc voltmeter,
   d. calculate \( V_{os} \) from

\[ V_{os} = \frac{R_3}{R_3 + R_7} V_{o2} \]  

(3)

2. **Open-loop differential-mode voltage gain** \( G_{vdm} \)
   a. close switches \( S_2 \) and \( S_4 \),
   b. set \( V_{ic} \) to zero by connecting pin 1 to ground,
   c. connect the output of the signal generator to pin 2 for \( V_{id} \),
   d. adjust \( R_p \) to change the dc value of \( V_{id} \) to get

\[ \Delta V_{id} = V_{id}(1) - V_{id}(2) \]  

(4)

e. measure the corresponding dc values of \( V_{o2} \) to get

\[ \Delta V_{o2} = V_{o2}(1) - V_{o2}(2) \]  

(5)

f. calculate \( G_{vdm} \) from

\[ G_{vdm} = \left( \frac{R_3}{R_5} \right) \left( \frac{R_7}{R_3 + R_7} \right) \frac{1}{\frac{\Delta V_{o2}}{\Delta V_{id}}} \]  

(6)

3. **Common-mode rejection ratio** CMRR
   a. close switches \( S_2 \) and \( S_4 \),
   b. set \( V_{id} \) to zero by connecting pin 2 to ground,
   c. connect the output of the signal generator to pin 1 for \( V_{ic} \),
   d. adjust \( R_p \) to change the dc value of \( V_{ic} \) to get

\[ \Delta V_{ic} = V_{ic}(1) - V_{ic}(2) \]  

(7)

e. measure the corresponding dc values of \( V_{o2} \) to get

\[ \Delta V_{o2} = V_{o2}(1) - V_{o2}(2) \]  

(8)
4. Positive input terminal current \( I_p \)
   a. open switch \( S_2 \), close switch \( S_4 \),
   b. set \( V_i \) and \( V_{id} \) to zero by connecting pins 1 and 2 to ground,
   c. measure \( V_{o2} \) with a dc voltmeter,
   d. calculate \( I_p \) from
   \[
   I_p = -\frac{1}{R_p} \left[ \frac{R_3}{R_3 + R_f} V_{o2} + V_{os} \right]
   \]
   \[
   \text{(10)}
   \]

5. Negative input terminal current \( I_n \)
   a. close switch \( S_2 \), open switch \( S_4 \),
   b. set \( V_i \) and \( V_{id} \) to zero by connecting pins 1 and 2 to ground,
   c. measure \( V_{o2} \) with a dc voltmeter,
   d. calculate \( I_n \) from
   \[
   I_n = \frac{1}{R_n} \left[ \frac{R_3}{R_3 + R_f} V_{o2} + V_{os} \right]
   \]
   \[
   \text{(11)}
   \]

6. Input bias current \( I_B \) and input bias offset current \( I_{BOS} \)
   a. calculate \( I_B \) and \( I_{BOS} \) from
   \[
   I_B = \frac{I_p + I_n}{2}
   \]
   \[
   I_{BOS} = I_p - I_n
   \]
   \[
   \text{(12)}
   \]

Example. Four 741-type op-amps were tested with this circuit. Circuit values for the DUT are given below.

\[
V_{CC} = 5.06V
\]
\[
V_{EE} = 5.05V
\]
\[
R_f = 51K\Omega
\]

<table>
<thead>
<tr>
<th>Data for ( V_{os} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>7001</td>
</tr>
<tr>
<td>7014A</td>
</tr>
<tr>
<td>2E23</td>
</tr>
<tr>
<td>D34</td>
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</table>
### Data for $G_{vdm}$

<table>
<thead>
<tr>
<th>Unit</th>
<th>$V_{id1}$ (V)</th>
<th>$V_{id2}$ (V)</th>
<th>$V_{oa1}$ (V)</th>
<th>$V_{oa2}$ (V)</th>
<th>$G_{vdm}$ (V/V)</th>
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</thead>
<tbody>
<tr>
<td>7001</td>
<td>-1.012</td>
<td>-0.316</td>
<td>+1.023</td>
<td>-0.276</td>
<td>26.00K</td>
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<tr>
<td>7014</td>
<td>-1.001</td>
<td>-0.258</td>
<td>+1.069</td>
<td>-0.221</td>
<td>28.59K</td>
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<td>2E23</td>
<td>-1.049</td>
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<td>+1.038</td>
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<td>D34</td>
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<td>+1.096</td>
<td>-0.0666</td>
<td>5.59M</td>
</tr>
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</table>

### Data for CMRR

<table>
<thead>
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<th>$V_{ic2}$ (V)</th>
<th>$V_{oc1}$ (V)</th>
<th>$V_{oc2}$ (V)</th>
<th>CMRR</th>
</tr>
</thead>
<tbody>
<tr>
<td>7001</td>
<td>-1.029</td>
<td>-1.294</td>
<td>+1.069</td>
<td>0.757</td>
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<tr>
<td>7014</td>
<td>-1.075</td>
<td>-1.301</td>
<td>+1.069</td>
<td>0.819</td>
<td>45.65K</td>
</tr>
<tr>
<td>2E23</td>
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<td>-1.162</td>
<td>+1.044</td>
<td>0.878</td>
<td>52.63K</td>
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<tr>
<td>D34</td>
<td>-1.018</td>
<td>1.065</td>
<td>+1.048</td>
<td>0.974</td>
<td>39.10K</td>
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I. Introduction
Instrumentation amplifiers (IA) are often referred to as ‘super op-amps’ in the electronics industry. IAs are applied in systems where accuracy and precision are required. This includes systems for industrial measurement and control, medical instrumentation, process monitoring, and low noise amplification, to name a few. In order to perform well in these systems, an instrumentation amplifier is designed to meet the following specifications –

- precise finite differential-mode gain $G_{vdm}$ in the range of 1 to 1,000,
- zero common-mode voltage gain $G_{vcm}$,
- infinite CMRR necessary to eliminate common-mode signals,
- infinite differential-mode and common-mode input impedance, and
- zero output impedance.

The electronic symbol for a typical IA is shown in Figure 1. The amplifier operates on a differential input voltage connected between the ±$V_{in}$ pins. The differential-mode voltage gain is set by a resistor connected to the gain set terminals. With the output sense pin connected to the output, a resistor in series with a variable voltage source are applied to increase the CMRR and to trim the input offset.

![Figure 1](IA_symbol.png)

II. Components and Instruments
A partial list of the components and instruments required for this lab are shown below.

**Components:**
- Op-amp: OP-07 (4)
- Potentiometer: 10K, trimpot (2)
- Resistors: assorted values

**Instruments:**
- Power supply: Agilent E3620A
- Multimeter: Agilent 34401A
- Function generator: Agilent 33120A
- Oscilloscope: Agilent 54621A
- Additional:
  - Breadboard
  - Tool box
  - Hook-up wire

III. The Three Op-Amp IA
A three op-amp instrumentation amplifier is constructed from a two op-amp differential amplifier coupled to a single op-amp difference amplifier as shown in Figure 2. The inputs to the IA are the differential-mode voltage $V_{id}$ and
the common-mode voltage $V_{ic}$. The IA output is the single-ended voltage $V_o$ which is a function of the mode voltages expressed as

$$V_o = \left[1 + \frac{R_2}{R_1}\right] \left[\frac{R_4}{R_3 + R_4}\right] - \frac{R_2}{R_1} V_{ic} + \frac{1}{2} \left[1 + \frac{R_2}{R_1}\right] \left[\frac{R_4}{R_3 + R_4}\right] \left[1 + \frac{2R_6}{R_G}\right] + R_2 \left[1 + \frac{2R_5}{R_G}\right] V_{id}$$

$$V_o = G_{Vcm} V_{ic} + G_{Vdm} V_{id}$$

where $G_{Vcm}$ and $G_{Vdm}$ define the common-mode and differential-mode voltage gains, respectively. For clarity, these gains are written as

$$G_{Vcm} = \left[1 + \frac{R_2}{R_1}\right] \left[\frac{R_4}{R_3 + R_4}\right] - \frac{R_2}{R_1}$$

$$G_{Vdm} = \frac{1}{2} \left[1 + \frac{R_2}{R_1}\right] \left[\frac{R_4}{R_3 + R_4}\right] \left[1 + \frac{2R_6}{R_G}\right] + R_2 \left[1 + \frac{2R_5}{R_G}\right]$$

For the ideal IA, it is necessary to match resistors with the following conditions

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

$$R_5 = R_6 = R$$

$$R_G = \text{gain setting resistor}$$

With these values, the voltage gains approach their ideal values of
\[ G_{Vcm} = \left( 1 + \frac{R_2}{R_1} \right) \left( \frac{R_4}{R_1 + R_4} \right) - \frac{R_2}{R_1} \rightarrow 0 \]

\[ G_{Vdm} = \frac{1}{2} \left[ \left( 1 + \frac{R_2}{R_1} \right) \left( \frac{R_4}{R_3 + R_4} \left( 1 + \frac{2R_6}{R_G} \right) + \frac{R_2}{R_1} \left( 1 + \frac{2R_5}{R_G} \right) \right) \right] \rightarrow \frac{R_2}{R_1} \left( 1 + \frac{2R_5}{R_G} \right) \]

(4)

With suitable values for all resistors, \( G_{Vdm} \) can be varied over a large range from unity to thousands with the gain-setting resistor \( R_6 \). The CMRR for this IA is determined from

\[ CMRR = 20\log_{10} \left( \frac{G_{Vdm}}{G_{Vcm}} \right) = 20\log_{10} \left( \frac{1}{2} \left[ \frac{1}{1 + \frac{R_2}{R_1}} \left( \frac{R_4}{R_3 + R_4} \left( 1 + \frac{2R_6}{R_G} \right) + \frac{R_2}{R_1} \left( 1 + \frac{2R_5}{R_G} \right) \right) \right] \right) \rightarrow \infty \]

(5)

Similar to the difference amplifier, the IA’s CMRR approaches an infinite value for perfectly balanced stages.

III. The Two Op-Amp IA

The schematic for the two op-amp instrumentation amplifier is shown in Figure 3. This IA design is more economical than the previous one in that it requires only two op-amps, four onboard resistors and one external gain-set resistor. Without the analysis details, the common-mode and differential-mode gains are expressed as

\[ G_{Vcm} = 1 - \frac{R_2R_1}{R_1R_4} \]

\[ G_{Vdm} = \frac{R_4}{R_3} + \frac{R_5}{R_G} \left( 1 + \frac{R_3}{R_5} \right) + \frac{1}{2} \left( 1 + \frac{R_2R_4}{R_1R_3} \right) \]

(6)
With \( R_4 = R_1 \) and \( R_3 = R_2 \), the common-mode gain approaches the ideal value of zero to allow an infinite CMRR. The differential-mode gain is controlled by the gain-setting resistor \( R_G \) and is written as

\[
G_{V_{dm}} = 1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G} 
\]

Unlike the three op-amp version, the gain range for this design does not have a lower limit of unity. From expressions for the differential and common mode gains, the CMRR is determined from

\[
CMRR = 20 \log_{10} \left( \frac{G_{V_{dm}}}{G_{V_{cm}}} \right) = 20 \log_{10} \left( \frac{R_G}{R_3} + \frac{R_3}{R_G} \left( 1 + \frac{R_2}{R_3} + \frac{1}{2} \left( 1 + \frac{R_2 R_4}{R_1 R_3} \right) \right) \right) \rightarrow \infty 
\]

IV. Experiment Procedure – Three Op-Amp IA

Design the three op-amp instrumentation amplifier shown again in Figure 4. The gain of the amplifier should range from 1 to 1000 and be adjustable with the resistor \( R_G \). Use OP07 operational amplifiers, ±5 volt supplies, and 1% resistors in your design. Prepare a written lab report which contains the items listed below.

(a) **Pre-lab:** A detailed description and schematic of your proposed design including equations for the components and their values. Provide a procedure for calibrating the amplifier which includes the independent adjustments of offset, CMRR, and voltage gain.

(b) **Lab:**

i. Build your IA design on a breadboard with –

   (1) a three-binding post breadboard,
   (2) tight layout of all components, and
   (3) the selection of resistors for matched values.

   Photos of circuit layout on a breadboard are shown in Figure 5.

ii. Calibrate your design for maximum CMRR and minimum offset \( V_{os} \).

iii. Test your IA in the lab and provide the following data:

   (1) the output voltage \( V_o \) with \( V_{sc} \) and \( V_{id} \) set to zero, and the gain set to 1, 10, 100, and 1000,
   (2) the CMRR with the gain set to 1, 10, 100, and 1000, and
   (3) a graph with a plot of voltage gain at 500Hz versus \( R_G \); specifically indicate on this plot data points for gains of 1, 10, 100 and 1000.

Prepare a schematic of your actual design and make comments on the accuracy of measured versus calculated values. Explain whether or not your calibration procedure is correct and actually works.
Figure 4
Three op-amp IA with CMRR and offset adjust

Figure 5
Breadboard layouts for the three op-amp IA
V. Experiment Procedure – Two Op-Amp IA

Design the two op-amp instrumentation amplifier. The gain of the amplifier should range from 2 to 1000 and be adjustable with the resistor $R_g$. Use OP07 operational amplifiers, ±5 volt supplies, and 1% resistors in your design. Prepare a written lab report which contains the items listed below.

(a) Pre-lab: A detailed description and schematic of your proposed design including equations for the components and their values. Provide a procedure for calibrating the amplifier which includes the independent adjustments of offset, CMRR, and voltage gain.

(b) Lab:
   i. Build your IA design on a breadboard with –
      (1) a three-binding post breadboard,
      (2) tight layout of all components, and
      (3) the selection of resistors for matched values.
   ii. Calibrate your design for maximum CMRR and minimum offset $V_{os}$.
   iii. Test your IA in the lab and provide the following data:
      (1) the output voltage $V_o$ with $V_i^c$ and $V_i^d$ set to zero, and the gain set to 1, 10, 100, and 1000,
      (2) the CMRR with the gain set to 2, 10, 100, and 1000, and
      (3) a graph with a plot of voltage gain versus $R_g$; specifically indicate on this plot data points for gains of 2, 10, 100 and 1000.

Prepare a schematic of your actual design and make comments on the accuracy of measured versus calculated values. Explain whether or not your calibration procedure is correct and actually works.
Lab Experiment No. 16
Linear Voltage Regulators

I. Introduction
Voltage regulators are important subcircuits in electronic power supply systems. As the name implies, these circuits are assigned the task of transforming an ill-precise and often fluctuating (unregulated) input voltage into a precise and constant (regulated) output voltage. This task is further complicated with the specification of the regulator to supply a substantial amount of output load current. A well-regulated and controlled power supply voltage is a fundamental requirement in almost all electronic systems. The subject of this lab exercise is to build and test voltage regulator circuits built from discrete components and integrated circuits. Make use of the parts supplied by the GTA and the instruments located on the lab bench to perform this experiment.

II. Components and Instruments
The components and instruments required for this lab are listed below.

Components:
- OP-07 (2)
- 2N3904 (2)
- 1N751A
- J175
- LM7805 (1)
- Capacitors: 0.01µF (2), 0.1µF, 0.33µF, 10µF (3)
- Resistors: (1/4W unless noted otherwise) 200Ω, 1KΩ, 3.3KΩ, 910Ω
- Potentiometer: 10K, trimpot (1)
- Load resistors: 39Ω (2W), 100Ω (1W), 200Ω (1/2W), 390Ω (2)

Instruments:
- Power supply (Agilent E3620A)
- Multimeter (Agilent 34401A)
- Additional:
  - Breadboard
  - Tool box
  - Hook-up wire

III. Voltage Regulator Design and Operation
The block diagram of a typical linear voltage regulator is shown in Figure 1. The input to the regulator is an unregulated external voltage $V_{\text{ext}}$ while the output is the regulated voltage $V_{\text{out}}$ applied to the load resistor $R_L$. For proper operation, $V_{\text{ext}}$ must be larger than $V_{\text{out}}$ by about 1.5V to 2V. The difference between $V_{\text{ext}}$ and $V_{\text{out}}$ is known as the dropout voltage $V_{\text{drop}}$. The regulator is basically a feedback circuit with a series pass element $Q_p$ (usually a transistor) controlled by an error amplifier (EA) in the feedback loop. The error amplifier compares a portion of $V_{\text{out}}$ ($V_f$) provided by the voltage divider $R_1$ and $R_2$ to a reference voltage $V_{\text{ref}}$ generated by a voltage reference circuit biased by current source $I_{\text{bias}}$. If the feedback voltage $V_f$ is less than $V_{\text{ref}}$, the error amplifier increases the drive current to $Q_p$ causing it to conduct or pass more current to the load. This, in turn, produces an increase in both $V_{\text{out}}$ and $V_f$. Otherwise, if $V_f$ is greater than $V_{\text{ref}}$, EA will reduce the drive current to $Q_p$ and less current will be passed to the load causing a decrease in $V_{\text{out}}$ and $V_f$. Assuming EA provides a substantial amount of gain around the feedback loop (large loop gain), $V_{\text{out}}$ is determined from

$$V_{\text{out}} = \left(1 + \frac{R_1}{R_2}\right)V_{\text{ref}} \quad (1)$$

As this expression illustrates, $V_{\text{out}}$ is a function of the reference voltage $V_{\text{ref}}$ and not a function of the input voltage $V_{\text{ext}}$. Since voltage reference circuits are not required to drive large loads, they can be designed with suitably biased Zener diodes and bandgap references to yield high levels of precision in $V_{\text{ref}}$. With such references, the regulator is quite capable of producing a precise and well-regulated output voltage $V_{\text{out}}$. 
IV. Regulator Characteristics

Voltage regulators are characterized with respect to their ability to maintain a constant output voltage in the presence of variations in the external supply voltage and the load resistor. Metrics for gauging this ability are generated by measuring the change in the output voltage with respect to changes in these components. The relative strength of these changes is formulated in terms of regulation factors known as line or input regulation and load or output regulation. By convention, line regulation is usually measured at a nominal value of load current and is defined as

$$\text{Line regulation} = \left. \frac{\Delta V_{out}}{\Delta V_{ext}} \right|_{I_L=I_L(nom)}$$

and expressed in mV/V. The small-scale version of line regulation is determined from the ratio of per unit changes in these voltages. This ratio is similar to that defined for current sources in a previous lab experiment which uses the $S_3$ sensitivity function where

$$S_3(V_{out}, V_{ext}) = \left. \frac{\Delta V_{out}}{\Delta V_{ext}} \right|_{V_{out}=V_{out}(nom)} = \left. \frac{V_{out}(nom)}{V_{ext}(nom)} \cdot \frac{\Delta V_{out}}{\Delta V_{ext}} \right|_{I_L=I_L(nom)}$$

$V_{ext}(nom)$ and $V_{out}(nom)$ are nominal values of the input and output voltages, respectively. Load regulation is defined as the ratio of the change in output voltage to a change in load current with a nominal value for the input voltage. That is,

$$\text{Load regulation} = \left. \frac{\Delta V_{out}}{\Delta I_L} \right|_{V_{ext}=V_{ext}(nom)}$$

which is expressed in mV/A. For small-signal variations in load current, the small-scale version of load regulation is calculated from

$$S_{LOAD}(V_{out}, I_L) = \left. \frac{\Delta V_{out}}{\Delta I_L} \right|_{I_L=I_L(nom)} = \left. \frac{V_{out}(nom)}{I_L(nom)} \cdot \frac{\Delta V_{out}}{\Delta I_L} \right|_{V_{ext}=V_{ext}(nom)}$$
In addition to these factors is the maximum power the series pass element can safely dissipate over the full range of regulator operation. Consider the NPN BJT shown in Figure 2 which is typically used as the series pass element \( Q_p \) in Figure 1. The dc power dissipated by \( Q_p \) (\( P_d \)) is the product of the collector-emitter voltage \( V_{CE} \) and the collector current \( I_C \).

The maximum power that \( Q_p \) must be capable of dissipating is determined from the maximum values for \( V_{ext} \) and \( I_L \), and the minimum value for \( V_{out} \). Since the collector current is approximately equal to the load current, \( P_d(\text{max}) \) is determined from

\[
P_d(\text{max}) = V_{CE}(\text{max}) \cdot I_C(\text{max}) = V_{ext}(\text{max}) - V_{out}(\text{min}) \cdot I_L(\text{max})
\]

Voltage regulators with a low value for the drop out voltage are known as low drop out (LDO) regulators which are designed to keep \( Q_p \)’s power dissipation as small as possible. In order to prevent catastrophic failure of the regulator, it is important to consider \( P_d(\text{max}) \) in the selection of the series pass element. Clearly, this device must be capable of dissipating this power without excessive heating that would cause failure. A common method to reduce excessive heating is to thermally connect the series pass element to a heat sink.

![Figure 2](image)

NPN BJT series pass element

V. Discrete Linear Voltage Regulator Design

The schematic of an adjustable linear voltage regulator is shown in Figure 3. A photo of the circuit breadboard is shown in Figure 4. This regulator is to be built with the discrete components shown on the schematic. Comparing the schematic to the block diagram in Figure 1, the blocks in the diagram listed below are identified with these components.

- \( I_{bias} \) and reference circuit – \( R_1, J_1, D_z, \text{OA}_1, R_2, \) and \( \text{RT}_1 \).
- Error amplifier EA – \( \text{OA}_2 \).
- Series pass element – \( Q_1, Q_2, R_3, \) and \( R_4 \).
- Feedback resistors – \( R_6 \) and \( R_7 \).
- Short circuit protection (not shown on the block diagram) – \( Q_3 \) and \( R_5 \).
- Decoupling capacitors (not shown on the block diagram) – \( C_1 \) through \( C_5 \).

(a) Design. Design this regulator by specifying the transistor \( Q_2 \), and calculating values for resistors \( R_1, R_5, R_6, \) and \( R_7 \) that will produce –

(i) a Zener diode bias current \( I_z \) within \( 2\text{mA} \leq I_z \leq 10\text{mA} \) over the range of \( V_{ext} \).  
(ii) an adjustable output voltage \( V_{out} \).  
(iii) a series pass transistor \( Q_2 \) capable of safely dissipating \( P_d(\text{max}) \), and  
(iv) the specifications listed in Table 1.

(b) Construction. Build your design on a breadboard following the breadboard layout shown in Figure 4.

(c) Measurement. Perform measurements necessary to obtain the following data.

(i) \( V_{out} \) adjustment range. 

(1) Set the input voltage to \( 15\text{V} \) for \( V_{ext}(\text{min}) \).

(2) Remove the load resistor for an open circuit output.

(3) Adjust the trimpot \( \text{RT}_1 \) over its full range, and measure the minimum and maximum values for \( V_{out} \); that is, \( V_{out}(\text{min}) \) and \( V_{out}(\text{max}) \).

(4) Place these values in Table 2 where indicated.

(5) Connect a \( 100\Omega \) load resistor at the output for \( R_L \) and repeat steps 3 and 4.

(6) Set the input voltage to \( 22\text{V} \) for \( V_{ext}(\text{max}) \) and repeat steps 2 through 5.
Table 1
Regulator specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{ext}}$</td>
<td>Input voltage</td>
<td>Supplied from an external unregulated ac adapter.</td>
<td>$15V \leq V_{\text{ext}} \leq 22V$</td>
</tr>
<tr>
<td>$I_{\text{ext}}$</td>
<td>Input current</td>
<td>Supplied from an external unregulated ac adapter.</td>
<td>$100mA \leq I_{\text{ext}} \leq 600mA$</td>
</tr>
<tr>
<td>$V_{\text{out}}$</td>
<td>Output voltage</td>
<td>$15V \leq V_{\text{ext}} \leq 22V$</td>
<td>$0V \leq V_{\text{out}} \leq 12V$</td>
</tr>
<tr>
<td>$R_L$</td>
<td>$R_L = \infty, 100\Omega$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{Lsc}}$</td>
<td>Short circuit output current</td>
<td>$15V \leq V_{\text{ext}} \leq 22V$</td>
<td>$0V \leq V_{\text{out}} \leq 12V$</td>
</tr>
<tr>
<td>$I_{\text{Lsc}}$</td>
<td>Short circuit output current</td>
<td>$V_{\text{out}} = 0V$</td>
<td>$500mA$</td>
</tr>
</tbody>
</table>

Figure 3
Adjustable discrete voltage regulator

Figure 4
Breadboard photo of the regulator
**Table 2**  
V<sub>out</sub> adjustment range (discrete design)

<table>
<thead>
<tr>
<th>R&lt;sub&gt;L&lt;/sub&gt; (Ω)</th>
<th>V&lt;sub&gt;ext&lt;/sub&gt;(min) = 15V</th>
<th>V&lt;sub&gt;ext&lt;/sub&gt;(max) = 22V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V&lt;sub&gt;out&lt;/sub&gt;(min) (V)</td>
<td>V&lt;sub&gt;out&lt;/sub&gt;(max) (V)</td>
</tr>
<tr>
<td>∞</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(ii) Line regulation.

1. Set the input voltage to 18V for V<sub>ext</sub>(nom).
2. Connect a 100Ω load resistor R<sub>L</sub> to the regulator output.
3. Adjust R<sub>T1</sub> for a nominal output voltage V<sub>out</sub>(nom) of 9V.
4. Calculate and measure the nominal load current I<sub>L</sub>(nom).
5. Sweep V<sub>ext</sub> from 15V to 22V and measure V<sub>out</sub> at each point in the sweep. Place measured values for these voltages in Table 3 where indicated.
6. Generate a plot of V<sub>out</sub> versus V<sub>ext</sub>. Use the measured values for this plot.
7. Calculate the large-scale line regulation (equation (2)) from the full range of V<sub>ext</sub> and V<sub>out</sub>.
8. Calculate the small-scale line regulation S<sub>3i</sub> (equation (3)).
9. Compare the two line regulation figures.

**Table 3**  
Line regulation (discrete design)  
(R<sub>L</sub> = 100Ω)

<table>
<thead>
<tr>
<th>V&lt;sub&gt;ext&lt;/sub&gt; (V) (specified)</th>
<th>V&lt;sub&gt;ext&lt;/sub&gt; (V) (measured)</th>
<th>V&lt;sub&gt;out&lt;/sub&gt; (V) (measured)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
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<td>17</td>
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<td>18</td>
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<td>19</td>
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<td>20</td>
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<tr>
<td>21</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>22</td>
<td>22</td>
<td>22</td>
</tr>
</tbody>
</table>

(iii) Load regulation.

1. Set the input voltage to 18V for V<sub>ext</sub>(nom).
2. Connect a 100Ω load resistor R<sub>L</sub> to the regulator output.
3. Adjust R<sub>T1</sub> for a nominal output voltage V<sub>out</sub>(nom) of 9V.
4. Calculate the nominal load current I<sub>L</sub>(nom).
5. Change R<sub>L</sub> from 900Ω to 39Ω and measure R<sub>L</sub> and V<sub>out</sub>. Calculate the load current I<sub>L</sub> and place these values in Table 4 where indicated.
6. Generate a plot of V<sub>out</sub> versus I<sub>L</sub>.
(7) Calculate the large-scale load regulation (equation (4)) from the full range of $I_L$ and $V_{out}$.

(8) Calculate the small-scale load regulation $S_3o$ (equation (5)).

(9) Compare the two load regulation figures.

<table>
<thead>
<tr>
<th>Table 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load regulation (discrete design)</td>
</tr>
<tr>
<td>( V_{ext} = 18V )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$R_L$ (Ω)</th>
<th>$R_L$ (Ω) (measured)</th>
<th>$V_{out}$ (V) (measured)</th>
<th>$I_L$ (A) (calculated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>900</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>390</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>100</td>
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<tr>
<td>78</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(iv) Short-circuit output current.

1. Remove the load resistor for an open circuit output.
2. Set the input voltage to 15V for $V_{ext}(\text{min})$.
3. Adjust $R_{T1}$ for a nominal output voltage $V_{out}(\text{nom})$ of 9V.
4. Short-circuit the regulator output by connecting a wire between the output terminals.
5. Measure and record the short-circuit output current $I_{Lsc}$.
6. Remove the wire and set the input voltage to 22V for $V_{ext}(\text{max})$.
7. Repeat steps 3 through 5.
8. Determine the maximum value recorded for $I_{Lsc}$ and save as $I_{Lsc}(\text{max})$.

(v) $P_d(\text{max})$.

1. Use the data in (iv) to calculate the maximum power $P_d(\text{max})$ dissipated in $Q_2$.

(d) Data sheet. Use the results calculated above to generate the regulator data sheet in Table 5.

<table>
<thead>
<tr>
<th>Table 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Discrete voltage regulator data sheet</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Range/value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{out}$</td>
<td>Adjustable output voltage range.</td>
<td>$V_{ext} = 15V$</td>
<td>$R_L = \infty$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 100\Omega$</td>
<td></td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>Adjustable output voltage range.</td>
<td>$V_{ext} = 22V$</td>
<td>$R_L = \infty$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 100\Omega$</td>
<td></td>
</tr>
</tbody>
</table>
ΔV_{\text{out}}/ΔV_{\text{ext}} & Line regulation. & 15V ≤ V_{\text{ext}} ≤ 22V \\
& & V_{\text{out}} = 9V \\
& & R_L = 100Ω \\
\hline
S_{3i} & Small-scale line regulation. & V_{\text{ext}} = 18V \\
& & V_{\text{out}} = 9V \\
& & R_L = 100Ω \\
\hline
ΔV_{\text{out}}/ΔI_L & Load regulation. & V_{\text{ext}} = 18V \\
& & V_{\text{out}} = 9V \\
& & 39Ω ≤ R_L ≤ 900Ω \\
\hline
S_{3o} & Small-scale load regulation. & V_{\text{ext}} = 18V \\
& & V_{\text{out}} = 9V \\
& & R_L = 100Ω \\
\hline
I_{\text{Lsc}}(\text{max}) & Maximum short circuit load current. & 15V ≤ V_{\text{ext}} ≤ 22V \\
& & V_{\text{out}} = 0V \\
& & 39Ω ≤ R_L ≤ 900Ω \\
\hline
P_d(\text{max}) & Maximum power dissipated by Q_2. & V_{\text{ext}} = 22V \\
& & V_{\text{out}} = 0V \\
& & I_L = I_{\text{Lsc}}(\text{max}) \\
\hline

VI. Integrated Circuit Voltage Regulator Design

An adjustable voltage regulator built from an LM7805 is shown in Figure 5. The LM7805 is a three-terminal integrated circuit (IC) voltage regulator with a regulated 5V output. By connecting the op-amp OA_1 and 10KΩ trimpot R_T to the IC as shown, it is possible to generate an adjustable output voltage. With V_{\text{ext}} in the range of 15V to 22V, V_{32} is held constant at 5V. However, this requires the voltage between pins 3 and 1 (V_{31}) to be greater than the drop-out voltage V_D which has a specified minimum value of 2V. By varying R_1 and R_2 through R_T, V_{\text{out}} is adjusted to keep V_{32} constant.

Assuming OA_1 has a large amount of open-loop gain, the expression for V_{\text{out}} is found from

$$V_{\text{out}} = \left( 1 + \frac{R_2}{R_1} \right) V_{32} = \left( 1 + \frac{R_2}{R_1} \right) 5V$$

(7)

The adjustable range of V_{\text{out}} is determined from

$$V_o(\text{min}) + 5V ≤ V_{\text{out}} ≤ V_{\text{ext}} - V_D$$

(8)

where V_o(\text{min}) is the minimum output voltage of OA_1. For example, with an input voltage V_{\text{ext}} of 18V and V_o(\text{min}) of 1.86V for the OP-07, V_{\text{out}} can be trimmed to have a value between 6.86V and 16V. Definition for line and load regulation, short-circuit output current, and P_d(max) apply to this design as well.

(a) **Design.** Design the regulator circuit shown in Figure 5 for an input voltage range between 15V and 22V; that is, 15V ≤ V_{\text{ext}} ≤ 22V.

(b) **Construction.** Build your design on a breadboard.

(c) **Measurement.** Perform measurements necessary to obtain the following data.

(i) V_{\text{out}} adjustment range.

(1) Set the input voltage to 15V for V_{\text{ext}}(\text{min}).

(2) Remove the load resistor for an open circuit output.

(3) Adjust the trimpot R_T, and measure the minimum and maximum values for V_{\text{out}}, that is, V_{\text{out}}(\text{min}) and V_{\text{out}}(\text{max}).

(4) Place these values in Table 6 where indicated.

(5) Connect a 100Ω load resistor at the output for R_L and repeat steps 3 and 4.
(6) Set the input voltage to 22V for $V_{\text{ext}}(\text{max})$ and repeat steps 2 through 5.

![Circuit Diagram](image)

**Figure 5**
Adjustable IC voltage regulator

| Table 6 |
|-----------------|-----------------|
| $V_{\text{out}}$ adjustment range (IC design) |
| $R_L$ (Ω) | $V_{\text{ext}}(\text{min}) = 15V$ | $V_{\text{ext}}(\text{max}) = 22V$ |
| $V_{\text{out}}(\text{min})$ (V) | $V_{\text{out}}(\text{max})$ (V) | $V_{\text{out}}(\text{min})$ (V) | $V_{\text{out}}(\text{max})$ (V) |
| $\infty$ | | | |
| 100 | | | |

(ii) Line regulation.
(1) Set the input voltage to 18V for $V_{\text{ext}}(\text{nom})$.
(2) Connect a 100Ω load resistor $R_L$ to the regulator output.
(3) Adjust $R_T$ for a nominal output voltage $V_{\text{out}}(\text{nom})$ of 9V.
(4) Calculate and measure the nominal load current $I_L(\text{nom})$.
(5) Sweep $V_{\text{ext}}$ from 15V to 22V and measure $V_{\text{out}}$ at each point in the sweep. Place measured values for these voltages in Table 7 where indicated.
(6) Generate a plot of $V_{\text{out}}$ versus $V_{\text{ext}}$. Use the measured values for this plot.
(7) Calculate the large-scale line regulation (equation (2)) from the full range of $V_{\text{ext}}$ and $V_{\text{out}}$.
(8) Calculate the small-scale line regulation $S_3$ (equation (3)).
(9) Compare the two line regulation figures.
Table 7
Line regulation (IC design)
\((R_L = 100\Omega)\)

<table>
<thead>
<tr>
<th>(V_{\text{ext}}) (V) (specified)</th>
<th>(V_{\text{ext}}) (V) (measured)</th>
<th>(V_{\text{out}}) (V) (measured)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
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<tr>
<td>17</td>
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<tr>
<td>18</td>
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<tr>
<td>21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(iii) Load regulation.

1. Set the input voltage to 18V for \(V_{\text{ext}}\) (nom).
2. Connect a 100\Ω load resistor \(R_L\) to the regulator output.
3. Adjust \(R_T\) for a nominal output voltage \(V_{\text{out}}\) (nom) of 9V.
4. Calculate the nominal load current \(I_L\) (nom).
5. Change \(R_L\) from 900\Ω to 39\Ω and measure \(R_L\) and \(V_{\text{out}}\). Calculate the load current \(I_L\) and place these values in Table 8 where indicated.
6. Generate a plot of \(V_{\text{out}}\) versus \(I_L\).
7. Calculate the large-scale load regulation (equation (4)) from the full range of \(I_L\) and \(V_{\text{out}}\).
8. Calculate the small-scale load regulation \(S_{30}\) (equation (5)).
9. Compare the two load regulation figures.

Table 8
Load regulation (IC design)
\((V_{\text{ext}} = 18\text{V})\)

<table>
<thead>
<tr>
<th>(R_L) (Ω) (measured)</th>
<th>(V_{\text{out}}) (V) (measured)</th>
<th>(I_L) (A) (calculated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>900</td>
<td></td>
<td></td>
</tr>
<tr>
<td>390</td>
<td></td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
(iv) Short-circuit output current.
   1. Remove the load resistor for an open circuit output.
   2. Set the input voltage to 15V for $V_{\text{ext}}(\text{min})$.
   3. Adjust $R_I$ for a nominal output voltage $V_{\text{out}}(\text{nom})$ of 9V.
   4. Short-circuit the regulator output by connecting a wire between the output terminals.
   5. Measure and record the short-circuit output current $I_{\text{Lsc}}$.
   6. Remove the wire and set the input voltage to 22V for $V_{\text{ext}}(\text{max})$.
   7. Repeat steps 3 through 5.
   8. Determine the maximum value recorded for $I_{\text{Lsc}}$ and save as $I_{\text{Lsc}}(\text{max})$.

(v) $P_d(\text{max})$.
   1. Use the data in (iv) to calculate the maximum power $P_d(\text{max})$ dissipated in the LM7805.

(d) Data sheet. Use the results calculated above to generate the regulator data sheet in Table 5.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Range/value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{out}}$</td>
<td>Adjustable output voltage range.</td>
<td>$V_{\text{ext}} = 15V$ $R_L = \infty$ $R_L = 100\Omega$</td>
<td>$\leq V_{\text{out}} \leq$</td>
</tr>
<tr>
<td>$V_{\text{out}}$</td>
<td>Adjustable output voltage range.</td>
<td>$V_{\text{ext}} = 22V$ $R_L = \infty$ $R_L = 100\Omega$</td>
<td>$\leq V_{\text{out}} \leq$</td>
</tr>
<tr>
<td>$\Delta V_{\text{out}}/\Delta V_{\text{ext}}$</td>
<td>Line regulation.</td>
<td>$15V \leq V_{\text{ext}} \leq 22V$ $V_{\text{out}} = 9V$ $R_L = 100\Omega$</td>
<td></td>
</tr>
<tr>
<td>$S_{3i}$</td>
<td>Small-scale line regulation.</td>
<td>$V_{\text{ext}} = 18V$ $V_{\text{out}} = 9V$ $R_L = 100\Omega$</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{\text{out}}/\Delta I_L$</td>
<td>Load regulation.</td>
<td>$V_{\text{ext}} = 18V$ $V_{\text{out}} = 9V$ $39\Omega \leq R_L \leq 900\Omega$</td>
<td></td>
</tr>
<tr>
<td>$S_{3o}$</td>
<td>Small-scale load regulation.</td>
<td>$V_{\text{ext}} = 18V$ $V_{\text{out}} = 9V$ $R_L = 100\Omega$</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{Lsc}}(\text{max})$</td>
<td>Maximum short circuit load current.</td>
<td>$15V \leq V_{\text{ext}} \leq 22V$ $V_{\text{out}} = 0V$</td>
<td></td>
</tr>
<tr>
<td>$P_d(\text{max})$</td>
<td>Maximum power dissipated by $Q_2$.</td>
<td>$V_{\text{ext}} = 22V$ $V_{\text{out}} = 0V$ $I_L = I_{\text{Lsc}}(\text{max})$</td>
<td></td>
</tr>
</tbody>
</table>
VII. Compare and Comment
(a) Compare the data sheet parameters listed in Table 5 and Table 9. Based on parameter differences, make a determination on which regulator is better for the processing of an unregulated input voltage
(b) Comment on which regulator is less expensive to build. Make use of component costs found in on-line catalogs.

VIII. References
Appendix 1  

Breadboard Layout Examples

EE 1105  
Bread board layout techniques  
September 13, 2008  
HTR, Jr.

Figure 1  
Resistor network schematic

Figure 2  
Wrong way – off the board with loops
**Figure 3**
Right way - low to the board and tight

**Figure 4**
Right way – low to the board and even tighter

- 155 -
Breadboard layout examples
HTR, Jr.
February, 25, 2009
Appendix 2

Lab Measurement Example

Lab Measurement Example 1

Figure 1
Network schematic

Figure 2
Breadboard layout
### Table 1
Voltage, current, and power map

<table>
<thead>
<tr>
<th>Element</th>
<th>Specified value</th>
<th>Measured value</th>
<th>Measured value (V)</th>
<th>Calculated value (A)</th>
<th>Element power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R₁</td>
<td>10KΩ</td>
<td>9.8251KΩ</td>
<td>+</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>R₂</td>
<td>3.3KΩ</td>
<td>3.2624KΩ</td>
<td>+</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>R₃</td>
<td>680Ω</td>
<td>684.22Ω</td>
<td>+</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>R₄</td>
<td>51KΩ</td>
<td>50.294KΩ</td>
<td>+</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>R₅</td>
<td>56KΩ</td>
<td>55.175KΩ</td>
<td>+</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>R₆</td>
<td>56KΩ</td>
<td>55.158KΩ</td>
<td>+</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>Vₚᵢ</td>
<td>10V</td>
<td>A</td>
<td>B</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 2
Kirchhoff current law

<table>
<thead>
<tr>
<th>Node</th>
<th>Total current into (Iₖᵢ) (A)</th>
<th>Total current out of (Iₖᵢₒ) (A)</th>
<th>KCL (Iₖᵢ − Iₖᵢₒ) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
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<td></td>
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<tr>
<td>3</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit</td>
<td>Total cw voltage drop ($V_{cw}$) (V)</td>
<td>Total ccw voltage drop ($V_{ccw}$) (V)</td>
<td>KVL ($V_{cw} - V_{ccw}$) (V)</td>
</tr>
<tr>
<td>------------------</td>
<td>-------------------------------------</td>
<td>----------------------------------------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>$V_{ps}$, $R_1$, $R_5$, $R_6$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_5$, $R_2$, $R_3$, $R_4$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ps}$, $R_1$, $R_2$, $R_3$, $R_4$, $R_6$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Lab Measurement Example 1

**Solutions**

![Network schematic](image1.png)

**Figure 1**
Network schematic

![Breadboard layout](image2.png)

**Figure 2**
Breadboard layout
### Table 1
Voltage, current, and power map

<table>
<thead>
<tr>
<th>Element</th>
<th>Specified value</th>
<th>Measured value</th>
<th>Element voltage</th>
<th>Element current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Nodes</td>
<td>Calculated value (A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+</td>
<td>−</td>
</tr>
<tr>
<td>R₁</td>
<td>10KΩ</td>
<td>9.8251KΩ</td>
<td>A</td>
<td>1</td>
</tr>
<tr>
<td>R₂</td>
<td>3.3KΩ</td>
<td>3.2624KΩ</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>R₃</td>
<td>680Ω</td>
<td>684.22Ω</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>R₄</td>
<td>51KΩ</td>
<td>50.294KΩ</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>R₅</td>
<td>56KΩ</td>
<td>55.175KΩ</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>R₆</td>
<td>56KΩ</td>
<td>55.158KΩ</td>
<td>2</td>
<td>B</td>
</tr>
<tr>
<td>Vₚs</td>
<td>10V</td>
<td>10.0147V</td>
<td>A</td>
<td>B</td>
</tr>
</tbody>
</table>

### Table 2
Kirchhoff current law

<table>
<thead>
<tr>
<th>Node</th>
<th>Total current into (Iᵢₙ) (A)</th>
<th>Total current out of (Iₒᵢₙ) (A)</th>
<th>KCL (Iᵢₙ − Iₒᵢₙ) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(Iᵢ₁) 111.1897µ</td>
<td>(Iᵢ₂ + Iᵢ₅) 111.1131µ</td>
<td>76.63n (0.069%)</td>
</tr>
<tr>
<td>2</td>
<td>(Iᵢ₄ + Iᵢ₅) 111.1766µ</td>
<td>(Iᵢ₆) 111.1117µ</td>
<td>64.91n (0.058%)</td>
</tr>
<tr>
<td>3</td>
<td>(Iᵢ₃) 55.64438µ</td>
<td>(Iᵢ₃) 56.06832µ</td>
<td>-423.9366n (0.762%)</td>
</tr>
<tr>
<td>4</td>
<td>(Iᵢ₂) 56.00478µ</td>
<td>(Iᵢ₃) 55.64438µ</td>
<td>360.4n (0.648%)</td>
</tr>
<tr>
<td>A</td>
<td>0</td>
<td>(Iᵢ₁ + Iᵢ₅) -210.3n</td>
<td>210.3n (0.189%)</td>
</tr>
<tr>
<td>B</td>
<td>(Iᵢ₅ + Iᵢ₆) -288.3n</td>
<td>0</td>
<td>-288.3nA (0.259%)</td>
</tr>
</tbody>
</table>
Table 3
Kirchhoff voltage law

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Total cw voltage drop ($V_{cw}$) (V)</th>
<th>Total ccw voltage drop ($V_{ccw}$) (V)</th>
<th>KVL ($V_{cw} - V_{ccw}$) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ps}, R_1, R_5, R_6$</td>
<td>($V_{R_1} + V_{R_5} + V_{R_6}$)</td>
<td>($V_{ps}$)</td>
<td>$-21.35m$ (0.208%)</td>
</tr>
<tr>
<td></td>
<td>10.26175</td>
<td>10.2831</td>
<td></td>
</tr>
<tr>
<td>$R_5, R_2, R_3, R_4$</td>
<td>($V_{R_2} + V_{R_3} + V_{R_4}$)</td>
<td>($V_{R_5}$)</td>
<td>$83\mu$ (0.0027%)</td>
</tr>
<tr>
<td></td>
<td>3.04068</td>
<td>3.0406</td>
<td></td>
</tr>
<tr>
<td>$V_{ps}, R_1, R_2, R_3, R_4, R_6$</td>
<td>($V_{R_1} + V_{R_2} + V_{R_3} + V_{R_4} + V_{R_6}$)</td>
<td>($V_{ps}$)</td>
<td>$-21.267m$ (0.207%)</td>
</tr>
<tr>
<td></td>
<td>10.26183</td>
<td>10.2831</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3
Oriented network schematic

Total power dissipated by resistors (delivered to resistors) = 1.14046mW
Total power delivered by the power supply = 1.145537mW
Absolute difference (%) = 5.076µW (0.445%)
Diode Characterization –

**Components:**
- Diode: 1N4148 (DUT)
- Resistors:
  - 200 (1/2 watt) 2K 20K 200K 2M
  - 330 (1/2 watt) 3.3K 33K 330K
  - 820 (1/2 watt) 8.2K 82K 820K
Diode Applications I –

Components:
Diodes:
   1N4148 (4)
Resistors:
   1KΩ  1.1KΩ  1.2KΩ
Capacitors:
   0.1μF  1.0μF  50μF
Diode Applications II –

Components:
Diode: 1N4148 (4)
Resistors: 330KΩ, 820KΩ, 1.0MΩ, 3.3MΩ, 4.7MΩ
Capacitors: 10nF (4), 0.1µF (4)
**BJT Device Characterization** –

Op-amp: OP-07  
NPN: 2N3904  
PNP: 2N3906  
Capacitors: 220pF (2)  
Resistors:  

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>51</td>
<td>(1/2W)</td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>(1/2W)</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510</td>
<td></td>
<td></td>
</tr>
<tr>
<td>820</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2K</td>
<td>(2)</td>
<td></td>
</tr>
<tr>
<td>3K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.1K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.2K</td>
<td>(2)</td>
<td></td>
</tr>
<tr>
<td>20K</td>
<td>(2)</td>
<td></td>
</tr>
<tr>
<td>30K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>51K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>82K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>200K</td>
<td>(3)</td>
<td></td>
</tr>
<tr>
<td>300K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2M</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
MOSFET Characterization –

Op-amp: OP-07 (2)
n-ch: ALD1103/n-ch
p-ch: ALD1103/p-ch

Capacitors: 220pF (2)

Resistors:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Value</th>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>68</td>
<td>1/2 watt</td>
<td>100</td>
<td>1/2 watt</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>2K</td>
<td></td>
<td>6.8K</td>
<td></td>
<td>20K</td>
<td>30K (2)</td>
</tr>
<tr>
<td>120K</td>
<td></td>
<td>200K</td>
<td></td>
<td>10K trimpot</td>
<td>68K</td>
</tr>
</tbody>
</table>
Self-Biased current Sinks and Sources –

NJFET: J11 (2)
PJFET: J176 (2)
Resistors:
470 820 1.2K 5.1K 9.1K
10K 15K
Biased Current Sinks and Sources –

<table>
<thead>
<tr>
<th>Component</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op-amp</td>
<td>TLC274</td>
</tr>
<tr>
<td>NPN BJT</td>
<td>2N3904 (4)</td>
</tr>
<tr>
<td>PNP BJT</td>
<td>2N3906 (4)</td>
</tr>
<tr>
<td>Diode</td>
<td>1N4148 (4)</td>
</tr>
<tr>
<td>Capacitors</td>
<td></td>
</tr>
<tr>
<td>220pF</td>
<td></td>
</tr>
<tr>
<td>10uF</td>
<td></td>
</tr>
<tr>
<td>Resistors</td>
<td></td>
</tr>
<tr>
<td>330</td>
<td></td>
</tr>
<tr>
<td>360</td>
<td></td>
</tr>
<tr>
<td>1K</td>
<td></td>
</tr>
<tr>
<td>7.5K</td>
<td></td>
</tr>
<tr>
<td>8.2K</td>
<td></td>
</tr>
<tr>
<td>9.1K</td>
<td></td>
</tr>
<tr>
<td>20K</td>
<td></td>
</tr>
</tbody>
</table>
**Current Mirrors –**

**Transistors –**
- NPN: 2N3904 (8)
- PNP: 2N3906 (8)
- NJFET: J113
- PJFET: J176

**Resistors:**
- 160Ω
- 330Ω (2)
- 620Ω
- 10KΩ
**Electronics Lab Exp 09 V2.0**

Bill of materials (BOM)

**BJT Bias Networks** –

**BJTs:**
NPN BJT: 2N3904
PNP BJT: 2N3906

**Resistors:**
200Ω  470Ω  620Ω  1KΩ  1.3KΩ  1.6KΩ  4.7KΩ  10KΩ  39KΩ  270KΩ  300KΩ  680KΩ  750KΩ
MOSFET Bias Networks –

MOSFETs:
- n and n-channel ALD1103

JFETs:
- NJFET J111
- PJFET J175

Resistors:
- 470Ω 680Ω 1KΩ 1.2KΩ
- 47KΩ 68KΩ

Others determined by students
Single Stage Amplifiers –

BJTs:
NPN BJT: 2N3904
PNP BJT: 2N3906

Capacitors:
10uF (2)  50uF

Resistors:
200Ω  470Ω  620Ω  1KΩ  1.3KΩ  1.6KΩ
4.7KΩ  10KΩ  39KΩ  270KΩ  300KΩ  680KΩ
750KΩ

Potentiometer:
1KΩ trim pot
## Operational Amplifier Design –

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>PJFET</td>
<td>J175 p-channel junction field effect transistor, plastic encapsulated</td>
<td>1</td>
</tr>
<tr>
<td>BJT</td>
<td>2N3904 NPN bipolar junction transistor, plastic encapsulated</td>
<td>11</td>
</tr>
<tr>
<td>BJT</td>
<td>2N3906 PNP bipolar junction transistor, plastic encapsulated</td>
<td>9</td>
</tr>
<tr>
<td>Resistor</td>
<td>270Ω, 1/4W, 5%, carbon film resistor</td>
<td>2</td>
</tr>
<tr>
<td>Resistor</td>
<td>390Ω, 1/4W, 5%, carbon film resistor</td>
<td>4</td>
</tr>
<tr>
<td>Resistor</td>
<td>560Ω, 1/4W, 5%, carbon film resistor</td>
<td>1</td>
</tr>
<tr>
<td>Resistor</td>
<td>1KΩ, 1/4W, 5%, carbon film resistor</td>
<td>3</td>
</tr>
<tr>
<td>Resistor</td>
<td>3.3KΩ, 1/4W, 5%, carbon film resistor</td>
<td>3</td>
</tr>
<tr>
<td>Resistor</td>
<td>5.1KΩ, 1/4W, 5%, carbon film resistor</td>
<td>2</td>
</tr>
<tr>
<td>Resistor</td>
<td>8.2KΩ, 1/4W, 5%, carbon film resistor</td>
<td>1</td>
</tr>
<tr>
<td>Resistor</td>
<td>10KΩ, 1/4W, 5%, carbon film resistor</td>
<td>5</td>
</tr>
<tr>
<td>Capacitor</td>
<td>120pF, NPO multilayer ceramic capacitor</td>
<td>1</td>
</tr>
</tbody>
</table>
Amplifier Networks –

The components and instruments required for this lab are listed below.

**Components:**

<table>
<thead>
<tr>
<th>Resistors</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>510Ω</td>
<td>3</td>
</tr>
<tr>
<td>5.1KΩ</td>
<td>2</td>
</tr>
<tr>
<td>10KΩ</td>
<td>5</td>
</tr>
<tr>
<td>18KΩ</td>
<td>2</td>
</tr>
<tr>
<td>20KΩ</td>
<td>2</td>
</tr>
<tr>
<td>30KΩ</td>
<td>2</td>
</tr>
<tr>
<td>39KΩ</td>
<td>2</td>
</tr>
<tr>
<td>51KΩ</td>
<td>2</td>
</tr>
<tr>
<td>others as needed</td>
<td>1</td>
</tr>
</tbody>
</table>
Op-Amp Test and Measurement –

**Active devices:**
- OP-07 op-amp (3)
- LM741 DUT

**Resistors:**
- 100Ω (2)
- 51KΩ (3)
- 2KΩ (5)
- 100KΩ (2)
- 30KΩ
- 10KΩ trimpot

**Capacitors:**
- 300nF, NPO multilayer
Instrumentation Amplifiers –

Active devices:
OP-07 (4)

Resistors:
Assorted, to be determined by students

Potentiometer:
10KΩ, trimpot (2)
Linear Voltage Regulator –

**Components:**
- OP-07 (2)
- 2N3904 (2)
- 1N751A
- J175
- LM7805

**Capacitors:**
- 0.01µF (2)
- 0.1µF
- 0.33µF
- 10µF (3)

**Resistors:**
- 200Ω
- 1KΩ
- 910Ω
- 3.3KΩ
- 39Ω (2W)
- 100Ω (1W)
- 200Ω (1/2W)
- 390Ω
- 1.8KΩ (2)

**Potentiometer:**
- 10K, trimpot