The circuit symbol for the $n$-channel enhancement MOSFET is illustrated in Figure 5.2. We discuss the basic operation of this device next.

**Operation in the Cutoff Region**

Consider the situation shown in Figure 5.3. Suppose that a positive voltage is applied to the drain relative to the source and that we start with $v_{GS} = 0$. Notice that $pn$ junctions appear at the drain-body and at the source-body interfaces. Virtually no current flows into the drain terminal, because the drain-body junction is reverse biased by the $v_{DS}$ source. This is called the **cutoff region** of operation. As $v_{GS}$ is increased, the device remains in cutoff until $v_{GS}$ reaches a particular value called the **threshold voltage** $V_{t}$. 

**Figure 5.3** For $v_{GS} < V_{t}$, the $pn$ junction between drain and body is reverse biased and $i_{D} = 0$. 

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Typically, the threshold voltage is one to a few volts. Thus, in cutoff, we have

\[ i_D = 0 \text{ for } V_{GS} \leq V_{th} \]  \hspace{1cm} (5.1)

**Operation in the Triode Region**

Now consider the situation illustrated in Figure 5.4, in which \( V_{GS} \) is greater than the threshold voltage. The electric field resulting from the applied gate voltage has repelled holes from the region under the gate and attracted electrons that can easily flow in the forward direction across the source–body junction. This simultaneous repulsion and attraction produces an \( n \)-type channel between the drain and the source. Then, when \( V_{DS} \) is increased, current flows into the drain, through the channel, and out of the source. For small values of \( V_{DS} \), the drain current is proportional to \( V_{DS} \). Furthermore, for

**Figure 5.4** For \( V_{GS} > V_{th} \), a channel of \( n \)-type material is induced in the region under the gate. As \( V_{GS} \) increases, the channel becomes thicker. For small values of \( V_{DS} \), \( i_D \) is proportional to \( V_{DS} \). The device behaves as a resistor whose value...
a given (small) value of $v_{DS}$, the drain current is also proportional to the excess gate voltage, $v_{GS} - V_n$.

Plots of $i_D$ versus $v_{DS}$ for several values of gate voltage are shown in Figure 5.4. In the triode region, the NMOS device behaves as a resistor connected between drain and source, but the resistance decreases as $v_{GS}$ increases.

Sometimes, circuit designers use FETs as voltage-controlled resistors. For example, we can design amplifiers in which the gain depends on a certain resistance value. By using a FET for the resistor, we can electrically control the gain of the amplifier. This principle is employed for automatic gain control (AGC) in radio receivers. AGC is particularly important for maintaining a nearly constant sound level in mobile situations, because the strength of a signal varies markedly as a vehicle moves about.

Now consider what happens if we continue to increase $v_{DS}$. Because of the current flow, the voltages between points along the channel and the source become greater as we move toward the drain. Thus, the voltage between gate and channel becomes smaller as we move toward the drain, resulting in a tapering of the channel thickness as illustrated in Figure 5.5. Because of the tapering of the channel, its resistance becomes larger with increasing $v_{DS}$, resulting in a lower rate of increase of $i_D$. In the triode region, the NMOS device behaves as a resistor connected between drain and source, but the resistance decreases as $v_{GS}$ increases.
For \( v_{DS} < v_{GS} - V_t \) and \( v_{GS} \geq V_t \), we say that the device is operating in the triode region, and the drain current is given by

\[
i_D = K \left[ 2(v_{GS} - V_t)v_{DS} - v_{DS}^2 \right]
\]

in which

\[
K = \left( \frac{W}{L} \right) \frac{KP}{2}
\]

As illustrated in Figure 5.1, \( W \) is the width of the channel and \( L \) is its length. The device parameter is

\[
KP = \mu_n C_{ox}
\]

in which \( \mu_n \) is the surface mobility of the electrons in the channel and \( C_{ox} \) is the capacitance of the gate per unit area. \( C_{ox} \), in turn, depends on the oxide thickness \( t_{ox} \). A typical value of \( KP \) for \( n \)-channel enhancement devices is 50 \( \mu A/V^2 \).

Usually, \( \mu_n \) and \( C_{ox} \) are determined by the fabrication process. However, in designing a circuit, we can vary the ratio \( W/L \) to obtain transistors best suited to various parts of the circuit.

**Operation in the Saturation Region**

We have seen that as \( v_{DS} \) is increased, the voltage between the gate and the drain end of the channel decreases. When the gate-to-drain voltage \( v_{GD} \) equals the threshold voltage \( V_t \), the channel thickness at the drain end becomes zero. For further increases in \( v_{DS} \), \( i_D \) is constant, as shown in Figure 5.5. This is called the saturation region, in which we have \( v_{GS} \geq V_t \) and \( v_{DS} \geq v_{GS} - V_t \) and the current is given by

\[
i_D = K(v_{GS} - V_t)^2
\]

Figure 5.6 shows the drain characteristics of an NMOS transistor.

![Figure 5.6](image)
Boundary Between the Triode and Saturation Regions

Next, we derive the equation for the boundary between the triode region and the saturation region in the $i_D - v_{DS}$ plane. This boundary exists when the channel thickness at the drain reaches zero, which occurs when $v_{GD} = V_t$. Thus, we want to find $i_D$ in terms of $v_{DS}$ under the condition that $v_{GD} = V_t$. Since $v_{GD} = v_{GS} - v_{DS}$, the condition at the boundary is

$$v_{GS} - v_{DS} = V_t$$  \hspace{1cm} (5.6)

Solving this equation for $v_{GS}$, substituting the result into Equation (5.5), and reducing, we have the desired boundary equation:

$$i_D = K v_D^2 $$  \hspace{1cm} (5.7)

Notice that the boundary between the triode region and the saturation region is a parabola.

Solving Equation (5.6) for $v_{GS}$ and substituting into Equation (5.5) also produces Equation (5.7). [Equations (5.2) and (5.5) give the same values for $i_D$ on the boundary.]

Given the values for $K_P$, $L$, $W$, and $V_t$, we can plot the static characteristics of an NMOS transistor.

Example 5.1  Plotting the Characteristics of an NMOS Transistor

A certain enhancement-mode NMOS transistor has $W = 160 \mu m$, $L = 2 \mu m$, $K_P = 50 \mu A/V^2$, and $V_t = 2 V$. Plot the drain characteristic curves to scale for $v_{GS} = 0, 1, 2, 3, 4,$ and $5 V$.

**SOLUTION**  First, we use Equation (5.3) to compute the device constant:

$$K = \left( \frac{W}{L} \right) \frac{K_P}{2} = 2 mA/V^2$$

Equation (5.7) gives the boundary between the triode region and the saturation region. Thus, we have

$$i_D = K v_D^2 = 2 v_D^2$$

where $i_D$ is in mA and $v_D$ is in volts. The plot of this equation is the dashed line shown in Figure 5.6.

Next, we use Equation (5.5) to compute the drain current in the saturation region for each of the $v_{GS}$ values of interest. We obtain

$$i_D = K (v_{GS} - V_t)^2 = 2(v_{GS} - 2)^2$$

where, again, the current is in mA. Substituting values, we have

- $i_D = 18 mA$ for $v_{GS} = 5 V$
- $i_D = 8 mA$ for $v_{GS} = 4 V$
- $i_D = 2 mA$ for $v_{GS} = 3 V$

and

- $i_D = 0 mA$ for $v_{GS} = 2 V$
For \( V_{GS} = 0 \) and 1 V, the device is in cutoff and \( i_D = 0 \). The preceding values are plotted in the saturation region as shown in Figure 5.6.

Finally, Equation (5.2) is used to plot the characteristics in the triode region. For each value of \( V_{GS} \), this equation plots as a parabola that passes through the origin (\( i_D = 0 \) and \( V_{DS} = 0 \)). The apex of each parabola is on the boundary between the triode region and the saturation region.

\[ \lambda \approx \frac{0.1}{L} \text{ V}^{-1} \]  

(5.8)

with \( L \) in \( \mu \text{m} \).

Next, we give the NMOS transistor equations, taking channel-length modulation into account. In cutoff (\( V_{GS} \leq V_{th} \))

\[ i_D = 0 \]  

(5.9)

In the triode region (\( V_{GS} \geq V_{th} \) and \( 0 \leq V_{DS} \leq V_{GS} - V_{th} \))

\[ i_D = K \left[ 2(V_{GS} - V_{th})v_{DS} - v_{DS}^2 \right] (1 + \lambda v_{DS}) \]  

(5.10)

In the saturation region (\( V_{GS} \geq V_{th} \) and \( V_{DS} \geq V_{GS} - V_{th} \))

\[ i_D = K(V_{GS} - V_{th})^2 (1 + \lambda v_{DS}) \]  

(5.11)

We can use SPICE to obtain plots of the characteristic curves for an NMOS transistor having given parameters.

**Example 5.2 Using SPICE to Plot Drain Characteristics**

Use SPICE to obtain a plot of the drain characteristics of a transistor having \( W = 160 \mu \text{m}, L = 2 \mu \text{m}, KP = 50 \mu \text{A/V}^2, \lambda = 0.05, \) and \( V_{th} = 2 \text{ V} \). Plot the drain characteristic curves to scale for \( V_{GS} = 0, 1, 2, 3, 4, \) and 5 V.
**Figure 5.7**
This circuit can be used to plot drain characteristics.

**SOLUTION**  First, we start Schematics and draw the circuit illustrated in Figure 5.7. Initially, we used the breakout part MbreakN3 for the NMOS transistor. To specify the model parameters, we first click on the NMOS symbol (it turns red), and then we use the `edit/model/edit instance model` command to bring up the window shown in Figure 5.8 and enter the model name (we used Mname) and the parameters shown, after which we click on OK. Then we double click on the NMOS symbol to bring up the window displayed in Figure 5.9, in which we enter the length and width values and click again on OK.

Next, we return to the main Schematics window and use the `analysis/setup/dc sweep` command to bring up the DC Sweep window shown in Figure 5.10a. We choose $v_{DS}$ as the main sweep variable and set up for a sweep from 0 to 10 V, in 0.1 V increments. Then we click on the Nested Sweep button to bring up the DC Nested Sweep window illustrated in Figure 5.10b, where we choose $v_{GS}$ as the variable and set up for a start value of 0, an end value of 5 V, and an increment of 1 V. Be sure to click on Enable Nested Sweep; a check will appear in the adjacent box.

**Figure 5.8** Model-editor window.
Then we use the `analysis/simulate` command to start the simulation, after which Probe starts and displays the characteristics shown in Figure 5.11. (We have attached a current marker to the drain of the NMOS to allow Probe to automatically plot the drain current after the simulation is finished.) The upward slope of the characteristics is due to the nonzero value of $\lambda$. Compare these characteristics to those of Figure 5.6, which are plots for the same parameters, except that $\lambda = 0$. 

![Figure 5.9 Attribute window for $M_1$.](image)

![Figure 5.10 DC-sweep setup windows.](image)
**Gate Protection**

Because of their construction, MOSFETs have extremely high input impedances between gate and channel—in excess of 1000 MΩ. In handling these devices, it is easy to develop static electric voltages greater than the breakdown voltage of the gate insulation. The breakdown of the insulating layer is destructive, usually resulting in a short circuit between gate and channel.

To alleviate this problem, the gate terminals can be protected by back-to-back Zener diodes as illustrated in Figure 5.12. If the device is exposed to a static electric charge, the Zener diodes break down, providing a nondestructive discharge path. The diodes are fabricated on the same chip as the FET. Often in ICs, gate protection takes the form of diodes connected from the input terminals to the power supply and ground terminals. (In normal operation, these diodes are reverse biased.) Protection diodes are not needed for devices internal to ICs that do not have direct external connections.

*Section summary:* In an NMOS transistor, when a sufficiently large (positive) voltage is applied to the gate relative to the source, electrons are attracted to the region under the gate, and a channel of n-type material is induced between the drain and the source. Then, if voltage is applied between the drain and the source, current flows into the drain, through the channel, and out of the source. Drain current is controlled by the voltage applied to the gate.


**EXERCISE**

5.1 Consider an NMOS having \( V_{th} = 2 \text{ V} \). What is the region of operation (triole, saturation, or cutoff) if (a) \( V_{GS} = 1 \text{ V} \) and \( V_{DS} = 5 \text{ V} \)? (b) \( V_{GS} = 3 \text{ V} \) and \( V_{DS} = 0.5 \text{ V} \)? (c) \( V_{GS} = 3 \text{ V} \) and \( V_{DS} = 6 \text{ V} \)? (d) \( V_{GS} = 5 \text{ V} \) and \( V_{DS} = 6 \text{ V} \)?

**Answer** (a) cutoff; (b) triode; (c) saturation; (d) saturation.

---

**EXERCISE**

5.2 Suppose that we have an NMOS transistor with \( KP = 50 \mu \text{A/V}^2 \), \( V_{th} = 1 \text{ V} \), \( \lambda = 0 \), \( L = 2 \mu \text{m} \), and \( W = 10 \mu \text{m} \). Sketch the drain characteristics for \( V_{DS} \), ranging from 0 to 10 \text{ V} \) and \( V_{GS} = 0, 1, 2, 3, \) and 4 \text{ V} \. Check your hand-drawn sketches by using SPICE to plot the characteristic curves.

**Answer** The circuit file is named Exer5.2 and can be found on the website.

---

5.2 **LOAD-LINE ANALYSIS OF A SIMPLE NMOS AMPLIFIER**

In this section, we analyze the NMOS amplifier circuit shown in Figure 5.13 by using the graphical load-line approach. The dc sources bias the MOSFET at a suitable operating point so that amplification of the input signal \( v_{in}(t) \) can take place. We will see that the input voltage \( v_{in}(t) \) causes \( V_{GS} \) to vary with time, which in turn causes \( I_D \) to vary. The changing voltage drop across \( R_D \) causes an amplified version of the signal to appear at the drain terminal.

Applying Kirchhoff’s voltage law to the input loop, we obtain the following expression:

\[
v_{GS}(t) = v_{in}(t) + V_{GG}
\]

\[(S.12)\]

![Figure 5.13](image-url)

**Figure 5.13**
Simple NMOS amplifier circuit.
As an example, we assume that the input signal is a 1-V peak, 1-kHz sinusoid and that $V_{GS}$ is 4 V. Then we have

$$v_{DS}(t) = \sin(2000\pi t) + 4 \quad (5.13)$$

Writing a voltage equation around the drain circuit, we obtain

$$V_{DD} = R_D i_D(t) + v_{DS}(t) \quad (5.14)$$

load-line equation.

For our example, we assume that $R_D = 1 \, \text{k}\Omega$ and $V_{DD} = 20 \, \text{V}$, so Equation (5.14) becomes

$$20 = i_D(t) + v_{DS}(t) \quad (5.15)$$

where we have assumed that $i_D(t)$ is in milliamperes. A plot of this equation on the drain characteristics of the transistor is a straight line called the load line.

To establish the load line, we first locate two points on it. Assuming that $i_D = 0$ in Equation (5.15), we find that $v_{DS} = 20 \, \text{V}$. These values plot as the lower right-hand end of the load line shown in Figure 5.14. For a second point, we assume that $v_{DS} = 0$, which yields $i_D = 20 \, \text{mA}$ when substituted into Equation (5.15). This pair of values ($v_{DS} = 0$ and $i_D = 20 \, \text{mA}$) plots as the upper left-hand end of the load line.

The operating point of an amplifier for a zero input signal is called the quiescent operating point, or Q-point. For $v_m(t) = 0$, Equation (5.12) yields $v_{GS} = V_{GO} = 4 \, \text{V}$. Therefore, the intersection of the curve for $v_{GS} = 4 \, \text{V}$ with the load line is the Q-point. The quiescent values are $I_{EQ} = 9 \, \text{mA}$ and $V_{DSQ} = 11 \, \text{V}$.

The maximum and minimum values of the gate-to-source voltage are $V_{GS_{\max}} = 5 \, \text{V}$ and $V_{GS_{\min}} = 3 \, \text{V}$. [See Equation (5.13).] In Figure 5.14, the intersections of the corresponding curves with the load line are labeled as points A and B, respectively. At

![Figure 5.14 Drain characteristics and load line for the circuit of Figure 5.13.](image-url)
point A, we find that $V_{DS\min} = 4$ V and $I_{D_{\text{max}}} = 16$ mA. At point B, we find that $V_{DS\max} = 16$ V and $I_{D_{\text{min}}} = 4$ mA.

A plot of $v_{DS}(t)$ versus time is shown in Figure 5.15. Notice that the peak-to-peak swing is 12 V, whereas the peak-to-peak swing of the input signal is 2 V. Furthermore, compared to the input signal, the ac voltage at the drain is inverted. (In other words, the positive peak of the input occurs at the same time as the minimum value of $v_{DS}$.)

Therefore, the circuit is an inverting amplifier. Apparently, the circuit has a voltage gain $A_v = -12 \text{ V}/2 \text{ V} = -6$, where the minus sign is due to the inversion.

Notice, however, that the output waveform displayed in Figure 5.15 is not a symmetrical sinusoid like the input. To illustrate, starting from the $Q$-point at $V_{DSQ} = 11$ V, the output voltage swings down to $V_{DS_{\min}} = 4$ V, for a change of 7 V. On the other hand, the output swings up to 16 V for a change of only 5 V from the $Q$-point on the positive-going half cycle of the output. We cannot properly define gain for the circuit, because the ac output signal is not proportional to the ac input. Nevertheless, the output signal is larger than the input, even if it is distorted.

In this circuit, the distortion is due to the fact that the characteristic curves for the FET are not uniformly spaced. If a much smaller input amplitude were applied, we would have amplification without appreciable distortion. This is true because the curves are more uniformly spaced if a very restricted region of the characteristics is considered. If we plotted the curves for 0.1-V increments in $v_{DS}$, the absence of distortion would be apparent.

The amplifier circuit we have analyzed in this section is fairly simple. Practical amplifier circuits are more difficult to analyze by graphical methods. Later in the chapter, we develop a linear small-signal equivalent circuit for the FET, and then we can use mathematical circuit-analysis techniques instead of graphical analysis. Usually, the equivalent-circuit approach is more useful for practical amplifier circuits. However, graphical analysis of simple circuits provides an excellent way to understand the basic concepts of amplifiers.
A DesignLab schematic of this circuit is found on the website in the file named Fig5.13. Use DesignLab to look at the various waveforms and become familiar with the operation of the circuit. You can learn much about electronics by using SPICE to play with circuits.

**EXERCISE**

5.3 Find $V_{DSQ}$, $V_{DS\min}$, and $V_{DS\max}$ for the circuit of Figure 5.13 if the circuit values are changed to $V_{DD} = 15$ V, $V_{GG} = 3$ V, $R_D = 1$ kΩ, and $v_m(t) = \sin(2000\pi t)$. The characteristics for the MOSFET are shown in Figure 5.14. Check your answers using a SPICE simulation. The parameters of the NMOS transistor are $K_P = 50 \, \mu A/V^2$, $V_T = 1$ V, $\lambda = 0$, $L = 10 \, \mu m$, and $W = 400 \, \mu m$.

**Answer** $V_{DSQ} \approx 11$ V, $V_{DS\min} \approx 6$ V, $V_{DS\max} \approx 14$ V. The circuit is stored in the file named Exer5.3, which can be found on the website.

### 5.3 BIAS CIRCUITS

The analysis of amplifier circuits is often undertaken in two steps. First, we analyze the dc circuit to determine the $Q$-point. In this analysis, the nonlinear device equations or the characteristic curves are used. Then, after the bias analysis is completed, we use a linear small-signal equivalent circuit to find the input resistance, voltage gain, and so on.

In integrated multistage amplifiers, the bias points of the various devices are interdependent. On the other hand, in discrete circuits, capacitors can be used to couple the stages, and the bias point for each stage can be established independently of the other stages. In this section, we consider the analysis and design of dc bias circuits suitable for RC-coupled discrete FET amplifiers, mainly to give you a better understanding of MOSFETs, biasing, and related concepts. The bias circuits discussed in the section are also applicable to JFETs. Later in the book, we will consider the more difficult problems associated with bias design for integrated circuits.

The two-battery bias circuit used in the amplifier of Figure 5.13 is not practical. Usually, only one dc voltage is readily available instead of two. However, a more significant problem is that FET parameters vary considerably from device to device. In general, we want to establish a $Q$-point near the middle of the load line, so that the output signal can swing in both directions without clipping. When the FET parameters vary from unit to unit, the two-battery circuit can wind up with some circuits biased near one end or the other.

**The Fixed-Plus Self-Bias Circuit**

The fixed-plus self-bias circuit illustrated in Figure 5.16a is a good discrete circuit for establishing $Q$-points that are relatively independent of device parameters.
Figure 5.16
Fixed- plus self-bias circuit.

For purposes of analysis, we replace the gate circuit with its Thévenin equivalent, as shown in Figure 5.16b. The Thévenin voltage is

\[ V_G = V_{DD} \frac{R_3}{R_1 + R_3} \]  

(5.16)

and the Thévenin resistance \( R_G \) is the parallel combination of \( R_1 \) and \( R_2 \). Writing a voltage equation around the gate loop of Figure 5.16b, we obtain

\[ V_G = v_{GS} + RslD \]  

(5.17)

(We have assumed that the voltage drop across \( R_G \) is zero, because the gate current of an NMOS transistor is extremely small.)

Usually, we want to bias the transistor in its saturation region, so we have

\[ i_D = K(v_{GS} - V_{th})^2 \]  

(5.18)

(To simplify bias-point analysis, we assume that \( \lambda = 0 \).)

The simultaneous solution of Equations (5.17) and (5.18) yields the operating point (provided that it falls in the saturation region). The larger root found for \( v_{DS} \) and the smaller root for \( i_D \) is the true operating point.
Example 5.3  Determination of Q-Point for the Fixed-Plus Self-Bias Circuit

Analyze the fixed-plus self-bias circuit shown in Figure 5.18. The transistor has $K P = 50 \mu A/V^2$, $V_{T0} = 2 V$, $\lambda = 0$, $L = 10 \mu m$, and $W = 400 \mu m$. Check your results by using SPICE.

SOLUTION  First, we use Equation (5.3) to compute the device constant:

$$K = \left( \frac{W}{L} \right) \frac{K P}{2} = 1 mA/V^2$$

**Figure 5.18**  Fixed-plus self-biased circuit of Example 5.3.
Substituting values into Equation (5.16), we have

\[
V_G = V_{DD} - \frac{R_2}{R_1 + R_2} = 20 - \frac{1}{(3 + 1)} = 5 \text{ V}
\]

The Q-point values must satisfy Equations (5.17) and (5.18). Thus, we need to find the solution of the pair of equations

\[
V_G = V_{GSQ} + R_s I_{DSQ}
\]

and

\[
I_{DSQ} = K(V_{GSQ} - V_{to})^2
\]

Using the last equation to substitute for \(I_{DSQ}\) in the expression for \(V_G\), we obtain

\[
V_G = V_{GSQ} + R_s K(V_{GSQ} - V_{to})^2
\]

Rearranging, we have

\[
V_{GSQ}^2 + \left(\frac{1}{R_s K} - 2V_{to}\right)V_{GSQ} + (V_{to})^2 - \frac{V_G}{R_s K} = 0
\]

After the values are substituted, we get

\[
V_{GSQ}^2 - 3.630V_{GSQ} + 2.148 = 0
\]

Solving, we find that \(V_{GSQ} = 2.886\) and \(V_{GSQ} = 0.744\). The second root is extraneous and should be discarded. Then we have

\[
I_{DSQ} = K(V_{GSQ} - V_{to})^2 = 0.784 \text{ mA}
\]

Solving for the drain-to-source voltage yields

\[
V_{DSQ} = V_{DD} - (R_D + R_S) I_{DSQ} = 14.2 \text{ V}
\]

which is high enough to ensure that operation is in saturation, as assumed in the solution.

To check our results by means of Schematics and PSpice, first we draw the circuit, utilizing the breakout part MbreakN3 for the MOSFET. Using the mouse to click on the MOSFET selects the MOSFET. Then we use the edit/model/edit instance model command to bring up the window in which we enter the device parameters \(KP = 50 \times 10^{-6}\), \(VTO = 2\) V, and \(LAMBDA = 0\). Returning to Schematics, we use the mouse to double click on the MOSFET to bring up the window in which we use \(L = 10 \times 10^{-6}\) and \(W = 400 \times 10^{-6}\).

Then we use the analysis/simulate command. After the simulation is finished, we use the analysis/examine output command to display the output file. Scrolling down, we find the results illustrated in Figure 5.19, which agree with our hand calculations within round-off error.
Design of the Fixed-Plus Self-Bias Circuit

Figure 5.20 shows graphical solutions of Equations (5.17) and (5.18) for several transistors with different values of $V_o$ and $K$. Notice that a higher value of $V_G$ (i.e., $V_{G2}$) results in less variation in $I_D$ between the high-current device and the low-current device, because the bias line becomes closer to horizontal. However, we cannot choose $V_G$ too high, because this raises the voltage drop across $R_S$, and sufficient voltage must be allocated for $V_{DSQ}$ and the drop across $R_D$.

![Graph of $I_D$ vs $V_{GS}$ and $V_{GS}$](image)

**Figure 5.20** The more nearly horizontal bias line results in less change in the $Q$-point.
The selection of the $Q$-point and the design of the bias circuit depend on the intended ac operation of the circuit. Later, we will see that in some amplifiers (for example, the common-source configuration) the output signal appears at the drain, and $R_D$ must assume a nonzero value. Then, a reasonable starting point for design is to select values such that

$$R_D I_DQ \approx V_{DD}/4$$  
$$V_{DSQ} \approx V_{DD}/2$$

and

$$R_S I_DQ \approx V_{DD}/4$$

implying that $R_S \approx R_D$.

On the other hand, in other amplifiers (in particular, the source follower, which we consider later in this chapter), we can design the bias circuit with $R_D = 0$. Then, a reasonable starting point for design is to select values such that

$$V_{DSQ} \approx V_{DD}/2$$

and

$$R_S I_DQ \approx V_{DD}/2$$

**Example 5.4 NMOS Bias-Circuit Design**

Design a fixed- plus self-bias circuit for a common-source NMOS amplifier. Nominaly, the transistor has $KP = 50 \mu A/V^2$, $W = 80 \mu m$, $L = 2 \mu m$, $\lambda = 0$, and $V_{dd} = 2 V$. The circuit is to have $V_{DD} = 20 V$ and $I_{DQ} \approx 2 mA$.

**SOLUTION** First we use Equation (5.3) to compute the device parameter:

$$K = \left( \frac{W}{L} \right) \frac{KP}{2} = 1 mA/V^2$$

For the design, we must specify values for $R_1$, $R_2$, $R_D$, and $R_S$. The design rules suggested for the common-source amplifier are

$$R_D I_DQ \approx V_{DD}/4$$

and

$$R_S I_DQ \approx V_{DD}/4$$

Treating these approximations as equations and solving them for $R_D$ and $R_S$, we find that

$$R_D = R_S = \frac{V_{DD}}{4I_{DQ}} = \frac{20 V}{4 \times 2 mA} = 2.5 k\Omega$$
In a discrete design, we need to select standard nominal values for the resistors. Usually, 5%-tolerance resistors are suitable for bias circuits. Thus, we choose

\[ R_D = R_S = 2.4 \, k\Omega \]

in this design.

The \( Q \) point values must satisfy the device equation

\[ I_{DQ} = K (V_{GSQ} - V_{P}) \]

Solving the equation for \( V_{GSQ} \) and substituting values, we obtain

\[ V_{GSQ} = V_D + \sqrt{\frac{I_{DQ}}{K}} = 2 + \sqrt{2} = 3.414 \, V \]

(\( V_{GSQ} = V_D - \sqrt{\frac{I_{DQ}}{K}} \) is an extraneous root.) Equation (5.17) must be satisfied by the \( Q \)-point values, so we have

\[ V_G = V_{GSQ} + R_S I_{DQ} = 3.414 + 2.4(2) = 8.214 \, V \]

Substituting values into Equation (5.16), we get

\[ V_G = V_{DD} \frac{R_2}{R_1 + R_2} \]

so that

\[ 8.214 = 20 \frac{R_2}{R_1 + R_2} \]

We now choose either \( R_1 \) or \( R_2 \). Usually, we want to use large values for these resistors to keep the current taken from the power supply small. Arbitrarily, we choose

\[ R_2 = 1 \, M\Omega \]

Then we can solve for \( R_1 \), obtaining \( R_1 = 1.435 \, M\Omega \). However, we want to use standard nominal values, so we select

\[ R_1 = 1.5 \, M\Omega \]

This completes the bias-circuit design.

\[ \square \]

**EXERCISE**

5.4 Analyze the circuit designed in Example 5.4. Check your results by using SPICE.

**Answer** \( I_{DQ} = 1.92 \, mA \), \( V_{GSQ} = 3.39 \, V \), \( V_{DSQ} = 10.8 \, V \). The circuit schematic is stored in the file named Exer5.4.
EXERCISE

5.5 Design a fixed-plus self-bias circuit for an NMOS source follower. Nominally, the transistor has \( K_F = 50 \mu A/V^2 \), \( W = 100 \mu m \), \( L = 2 \mu m \), \( \lambda = 0 \), and \( V_{ds} = 1 \) V. The circuit is to have \( V_{dd} = 15 \) V and \( I_{dq} \approx 2 \) mA. Use SPICE to check that your design provides a Q-point close to the desired value.

Answer We should choose \( R_D = 0 \) for a source follower. Many values will work for the other resistors. A reasonable set of values is \( R_S = 3.9 \) k\( \Omega \), \( R_1 = 1 \) M\( \Omega \), and \( R_2 = 2 \) M\( \Omega \). These values yield \( I_{dq} = 1.96 \) mA and \( V_{dsq} = 7.26 \) V.

5.4 SMALL-SIGNAL EQUIVALENT CIRCUITS

In the preceding section, we considered discrete dc bias circuits for FET amplifiers. Now we consider the relationships between signal currents and voltages resulting in small changes from the Q-point. As usual, we denote total quantities by lowercase letters with uppercase subscripts, such as \( i_D(t) \) and \( v_{gs}(t) \). The dc Q-point values are denoted by uppercase letters with an additional Q subscript, such as \( I_{dq} \) and \( V_{gsQ} \). The signals are denoted by lowercase letters with lowercase subscripts, such as \( i_d(t) \) and \( v_{gs}(t) \). The total current or voltage is the sum of the Q-point value and the signal. Thus, we can write

\[
i_D(t) = I_{dq} + i_d(t)
\]

and

\[
v_{gs}(t) = V_{gsQ} + v_{gs}(t)
\]

Figure 5.21 illustrates the terms in Equation (5.20).

In the following discussion, we assume that the FETs are biased in the saturation region, which is usually the case for amplifier circuits. Equation (5.5), repeated here for convenience, gives the total drain current in terms of the total gate-to-source voltage:

\[
i_D = K(v_{gs} - V_{io})^2
\]

![Figure 5.21](image)

Illustration of the terms in Equation (5.20).
Using Equations (5.20) and (5.21) to substitute into Equation (5.5), we obtain

\[ I_{DQ} + i_d(t) = K \left[ V_{GSQ} + v_{gs}(t) - V_{to} \right]^2 \]  

(5.22)

The right-hand side of Equation (5.22) can be expanded to get

\[ I_{DQ} + i_d(t) = K(V_{GSQ} - V_{to})^2 + 2K(V_{GSQ} - V_{to})v_{gs}(t) + Kv_{gs}^2(t) \]  

(5.23)

However, the Q-point values are also related by Equation (5.5), so that we have

\[ I_{DQ} = K(V_{GSQ} - V_{to})^2 \]  

(5.24)

Therefore, the first term on each side of Equation (5.23) can be canceled. Furthermore, we are interested in small-signal conditions for which the last term on the right-hand side of Equation (5.23) is negligible and can be dropped [i.e., we assume that \(|v_{gs}(t)|\) is much smaller than \(|(V_{GSQ} - V_{to})|\)]. With these changes, Equation (5.23) becomes

\[ i_d(t) = 2K(V_{GSQ} - V_{to})v_{gs}(t) \]  

(5.25)

If we define the transconductance of the FET as

\[ g_m = 2K(V_{GSQ} - V_{to}) \]  

(5.26)

Equation (5.25) can be written as

\[ i_d(t) = g_m v_{gs}(t) \]  

(5.27)

The gate current for the FET is negligible, so that we have

\[ i_g(t) = 0 \]  

(5.28)

Equations (5.27) and (5.28) can be represented by the small-signal equivalent circuit illustrated in Figure 5.22. Thus, for small signals, the FET is modeled by a voltage-controlled current source connected between the drain and source terminals. The model has an open circuit between gate and source.

**Figure 5.22**
Small-signal equivalent circuit for FETs.
Dependence of Transconductance on Q-Point and Device Parameters

We will see that the transconductance $g_m$ is an important parameter in the design of amplifier circuits. In general, better performance is obtained with higher values of $g_m$. Thus, designers need to know how Q-point and device parameters influence transconductance.

Solving Equation (5.24) for the quantity $(V_{GSQ} - V_{th})$ and substituting the results into Equation (5.26), we obtain

$$g_m = 2\sqrt{K T D_Q}$$  \hspace{1cm} (5.29)

An important point to notice is that $g_m$ is proportional to the square root of the Q-point drain current. Accordingly, we can increase $g_m$ by choosing a higher value of $I_{DQ}$.

If we use Equation (5.3) to substitute for $K$ in Equation (5.29), we obtain

$$g_m = \sqrt{2K P} \sqrt{W/L} \sqrt{I_{DQ}}$$  \hspace{1cm} (5.30)

Then, by using Equation (5.4) to substitute for $KP$, we have

$$g_m = \sqrt{2 \mu C_{ox} V_{th}} \sqrt{W/L} \sqrt{I_{DQ}}$$  \hspace{1cm} (5.31)

Thus, we can obtain higher values of $g_m$ for a given value of $I_{DQ}$ by increasing the width-to-length ratio of the MOSFET. Because process limitations place a minimum value on $L$, high $g_m$ implies large values for $W$. High transconductance is obtained at the cost of chip area.

More Complex Equivalent Circuits

Sometimes, additions to the equivalent circuit are needed to accurately model FETs. For example, we will need to include small capacitances between the device terminals when we consider the high-frequency response of FET amplifiers. The device equations and the equivalent circuit that we have derived from them describe only the static behavior of the device. For an accurate model with rapidly changing currents and voltages, capacitances are required.

Furthermore, the first-order equations we have used to obtain the equivalent circuit for the FET did not account for the small effect of $V_{DS}$ on the drain current, because we assumed that $\lambda = 0$. In other words, we assumed that the drain characteristics are horizontal in the saturation region, but this is not exactly true—the drain characteristics slope slightly upward with increasing $V_{DS}$. If we wish to account for the effect of $V_{DS}$ in the small-signal equivalent circuit, we must add a resistance $r_d$, called the drain resistance, between drain and source, as shown in Figure 5.23. In this case, Equation (5.27) becomes

$$i_d = \frac{g_m v_{gs} + v_{ds}}{r_d}$$  \hspace{1cm} (5.32)
Figure 5.23
FET small-signal equivalent circuit that accounts for the dependence of $i_D$ on $v_{DS}$.

Transconductance and Drain Resistance as Partial Derivatives

An alternative definition of $g_m$ can be found by examining Equation (5.32). Notice that if $v_{ds} = 0$, $g_m$ is the ratio of $i_d$ to $v_{gs}$. Mathematically, we obtain

$$g_m = \left. \frac{i_d}{v_{gs}} \right|_{v_{ds}=0}$$ \hspace{1cm} (5.33)

However, $i_d$, $v_{gs}$, and $v_{ds}$ represent small changes from the $Q$-point. Therefore, the condition $v_{ds} = 0$ is equivalent to requiring $v_{DS}$ to remain constant at the $Q$-point value, namely, $V_{DSS}$. Thus, we can write

$$g_m \approx \frac{\Delta i_D}{\Delta v_{GS}} \bigg|_{v_{DS}=V_{DSS}}$$ \hspace{1cm} (5.34)

where $\Delta i_D$ is an increment of drain current, centered at the $Q$-point. Similarly, $\Delta v_{GS}$ is an increment of gate-to-source voltage, centered at the $Q$-point.

Equation (5.34) is an approximation to a partial derivative. Therefore, $g_m$ is the partial derivative of $i_D$ with respect to $v_{GS}$, evaluated at the $Q$-point:

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{Q\text{-point}}$$ \hspace{1cm} (5.35)

Similarly, the reciprocal of the drain resistance is

$$\frac{1}{r_d} \approx \frac{\Delta i_D}{\Delta v_{DS}} \bigg|_{v_{GS}=V_{GSS}}$$ \hspace{1cm} (5.36)

Hence, we can write

$$\frac{1}{r_d} = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_{Q\text{-point}}$$ \hspace{1cm} (5.37)

Given the drain characteristics, we can determine approximate values of the partial derivatives for a specific $Q$-point. Then we can model the FET by its small-signal equivalent in the analysis of an amplifier circuit and use the values found for $g_m$ and $r_d$ to compute amplifier gains and impedances. In the next several sections, we present examples of this process. First, we show how to determine the values of $g_m$ and $r_d$, starting from the characteristic curves.

Example 5.5 Determination of $g_m$ and $r_d$ from the Characteristic Curves

Determine the values of $g_m$ and $r_d$ for the MOSFET having the characteristics illustrated in Figure 5.24 at a $Q$-point defined by $V_{GSS} = 3.5$ and $V_{DSS} = 10$ V.
**Figure 5.24** Determination of $g_m$ and $r_d$. See Example 5.5.

**SOLUTION** First, we locate the $Q$-point as shown in the figure. Then we use Equation (5.34) to find $g_m$:

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}} \bigg|_{v_{GS}=V_{DSQ}=10 \text{ V}}$$

We must make changes around the $Q$-point, while holding $v_{DS}$ constant at 10 V. Thus, the incremental changes are made along a vertical line through the $Q$-point. To obtain a representative value for $g_m$, we consider an increment centered on the $Q$-point (rather than making the changes in one direction from the $Q$-point). Taking the changes starting from the curve below the $Q$-point and ending at the curve above the $Q$-point, we have $\Delta i_D = 10.7 - 4.7 = 6 \text{ mA}$ and $\Delta v_{GS} = 1 \text{ V}$. This increment is labeled in the figure. Thus, we have

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}} = \frac{6 \text{ mA}}{1 \text{ V}} = 6 \text{ mS}$$

The drain resistance is found by applying Equation (5.36):

$$\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}} \bigg|_{v_{DS}=V_{DSQ}}$$

Because the incremental changes are to be made while holding $v_{GS}$ constant, the changes are made along the characteristic curve through the $Q$-point. Therefore, $1/r_d$ is the slope of the curve through the $Q$-point. For $v_{GS} = V_{GSQ} = 3.5 \text{ V}$, we
obtain \( i_D \approx 6.7 \text{ mA} \) at \( v_{DS} = 4 \text{ V} \) and \( i_D \approx 8.0 \text{ mA} \) at \( v_{DS} = 14 \text{ V} \). Accordingly, we obtain

\[
\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}} \approx \frac{(8.0 - 6.7) \text{ mA}}{(14 - 4) \text{ V}} = 0.13 \times 10^{-3} \text{ S}
\]

Taking the reciprocal, we find that \( r_d = 7.7 \text{ k}\Omega \).

---

**EXERCISE**

5.6 Find the values of \( g_m \) and \( r_d \) for the characteristics of Figure 5.24 at a \( Q \)-point of \( V_{GSQ} = 2.5 \text{ V} \) and \( V_{DSQ} = 6 \text{ V} \).

**Answer** \( g_m \approx 3.3 \text{ mS} \) and \( r_d \approx 20 \text{ k}\Omega \).

---

**EXERCISE**

5.7 Show that Equation (5.26) results from applying Equation (5.35) to Equation (5.5).

---

### 5.5 THE COMMON-SOURCE AMPLIFIER

The circuit diagram of a common-source amplifier is shown in Figure 5.25. The ac signal to be amplified is \( v(t) \). The coupling capacitors \( C_1 \) and \( C_2 \), as well as the bypass capacitor \( C_5 \), are intended to have very small impedances for the ac signal. In this section, we carry

![Common-source amplifier circuit diagram](image_url)  

**Figure 5.25** Common-source amplifier.
out a midband analysis in which we assume that these capacitors are short circuits for
the signal. Later, when we consider the frequency response of amplifiers, we include the
capacitors. The resistors \( R_1, R_2, R_3, \) and \( R_D \) form the bias network, and their values
are selected to obtain a suitable \( Q \)-point. The amplified output signal is applied to the
load \( R_L \).

**The Small-Signal Equivalent Circuit**

The small-signal equivalent circuit for the amplifier is illustrated in Figure 5.26. The
input coupling capacitor \( C_1 \) has been replaced by a short circuit. The MOSFET has been
replaced by its small-signal equivalent. Because the bypass capacitor \( C_3 \) is assumed to
be a short circuit, the source terminal of the FET is connected directly to ground—which
is why the circuit is called a common-source amplifier.

The dc supply voltage source acts as a short circuit for the ac signal. (Even if ac
current flows through the dc source, the ac voltage across it is zero. Thus, for ac signals,
the dc voltage source is a short.) Consequently, both \( R_1 \) and \( R_2 \) are connected from gate
to ground in the equivalent circuit. Similarly, \( R_D \) is connected from drain to ground.

**Voltage Gain**

Next, we derive an expression for the voltage gain of the common-source amplifier.
Referring to the small-signal equivalent circuit, we notice that the resistances \( r_d, R_D, \)
and \( R_L \) are in parallel. We denote the equivalent resistance by

\[
R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} \tag{5.38}
\]

The output voltage is the product of the current from the controlled source and the
equivalent resistance:

\[
v_o = -(g_m v_{gr}) R'_L \tag{5.39}
\]

The minus sign is needed because of the reference directions selected (i.e., the current
\( g_m v_{gr} \) flows out of the positive end of the voltage reference for \( v_o \)). Furthermore, the
input voltage and the gate-to-source voltage are equal:

\[
v_{in} = v_{gr} \tag{5.40}
\]

![Figure 5.26 Small-signal equivalent circuit for the common-source amplifier.](image)
Now, if we divide the respective sides of Equation (5.39) by those of Equation (5.40), we obtain the voltage gain:

\[ A_v = \frac{v_o}{v_{in}} = -g_m R'_L \]  

(5.41)

The minus sign in the expression for the voltage gain shows that the common-source amplifier is inverting. Notice that the voltage gain is proportional to \( g_m \).

**Input Resistance**

The input resistance of the common-source amplifier is given by

\[ R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 || R_2 \]  

(5.42)

The resistances \( R_1 \) and \( R_2 \) form part of the bias network, but their values are not critical. (See Section 5.3 for a discussion of the bias circuit.) Practical values range up to perhaps 10 M\( \Omega \) in circuits with discrete components. Thus, we have a great deal of freedom in designing the input resistance of a common-source amplifier. This is not true for BJT amplifier circuits.

**Output Resistance**

To find the output resistance of an amplifier, we disconnect the load, replace the signal source by its internal resistance, and then find the resistance seen looking into the output terminals. The equivalent circuit with these changes is displayed in Figure 5.27.

Because there is no source connected to the input side of the circuit, we conclude that \( v_{gs} = 0 \). Therefore, the controlled current source \( g_m v_{gs} \) produces zero current and appears as an open circuit. Consequently, the output resistance is the parallel combination of \( R_D \) and \( r_d \):

\[ R_o = \frac{1}{1/R_D + 1/r_d} \]  

(5.43)

**Example 5.6  Gain and Impedance of a Common-Source Amplifier**

Consider the common-source amplifier illustrated in Figure 5.28. The NMOS transistor has \( k_p = 50 \mu A/\sqrt{V} \), \( V_{th} = 2 V \), \( \lambda = 0 \), \( L = 10 \mu m \), and \( W = 400 \mu m \).
Find the midband voltage gain, input resistance, and output resistance of the amplifier. Then, if the input source is given by

\[ v(t) = 100 \sin(2000\pi t) \text{ mV} \]

compute the output voltage. Assume that the frequency of the source (which is 1000 Hz) is in the midband region.

**SOLUTION** First, we need to find the Q-point so that we can determine the value of \( g_m \) for the MOSFET. The bias circuit consists of \( R_1, R_2, R_D, \) and \( R_S, \) and the MOSFET. This circuit was analyzed in Example 5.3, where we determined that \( I_{DQ} = 0.784 \text{ mA}. \)

Next, we use Equation (5.30) to find the transconductance of the device:

\[ g_m = \sqrt{2KP} \sqrt{W/L} \sqrt{I_{DQ}} = 1.77 \text{ mS} \]

Because we have \( \lambda = 0, \) the drain characteristics are horizontal in the saturation region, and \( r_d = \infty. \)

Now we use Equations (5.38), (5.41), (5.42), and (5.43) to find

\[ R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} = 3197 \Omega \]

\[ A_v = \frac{v_{OC}}{v_{iN}} = -g_m R'_L = -5.66 \]

\[ R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 || R_2 = 750 \text{ k}\Omega \]

and

\[ R_o = \frac{1}{1/R_D + 1/r_d} = 4.7 \text{ k}\Omega \]
The signal voltage divides between the internal source resistance and the input resistance of the amplifier. Thus, we have

\[ v_{in} = v(t) \frac{R_{in}}{R + R_{in}} = 88.23 \sin(2000 \pi t) \text{ mV} \]

Then the output voltage can be found as

\[ v_o(t) = A_v v_{in}(t) = -500 \sin(2000 \pi t) \text{ mV} \]

Notice the phase inversion of \( v_o(t) \) compared with \( v_{in}(t) \).

**Example 5.7 SPICE Analysis of a Common-Source Amplifier**

Perform a transient analysis with PSpice to verify the result found for the output voltage in Example 5.6. Also, use an ac sweep to obtain a plot of the voltage-gain magnitude versus frequency to verify that 1000 Hz is in the midband region.

**SOLUTION** First we use Schematics to draw the circuit as shown in Figure 5.28. Next, we double click on the input source to bring up the window illustrated in Figure 5.29. For the ac analysis, we specify a source amplitude of AC = 100 mV. For the transient analysis, we enter the parameters VOFF = 0, VAMPL = 100 mV, and FREQ = 1000.

We set up the MOSFET parameters exactly as we did in Example 5.3. Then we use the analysis/setup/ac sweep command to bring up the window displayed in Figure 5.30a, in which we enter the parameters shown. Next, we use the analysis/setup/transient command to bring up the window shown in Figure 5.30b, in which we entered the parameters for the transient analysis.

![Setup window for the signal source.](image-url)
Figure 5.30 Analysis setup windows.

Now we use the `analysis/simulate` command to start the simulation, after which Probe starts. First, we look at the results of the transient analysis, which are shown in Figure 5.31. As expected, the output voltage is a 500-mV peak sine wave that is inverted compared with the input signal.

Next, we use the `plotfac` command in Probe to look at the ac sweep results. The gain magnitude $|V_{out}/V_{in}|$ is illustrated in Figure 5.32. We see that the gain magnitude is nearly constant upward from about 100 Hz. Thus, 1000 Hz is indeed in the midband range. Below 100 Hz, the gain magnitude declines because of

![Figure 5.31](image)

**Figure 5.31** $v_b(t)$ and $v_{in}(t)$ versus time for the common-source amplifier of Figure 5.28.
Figure 5.32 Gain magnitude versus frequency for the common-source amplifier of Figure 5.28.

the coupling and bypass capacitors. (We will consider the frequency response of amplifiers and how to choose the capacitor values later.)

EXERCISE

5.8 Find the voltage gain of the amplifier of Example 5.6 if \( R_L \) is replaced by an open circuit.

Answer \( A_{vo} = -8.32 \).

EXERCISE

5.9 Consider the circuit of Figure 5.25 with the bypass capacitor \( C_S \) replaced by an open circuit. Draw the small-signal equivalent circuit. Then, assuming, for simplicity, that \( r_d \) is an open circuit, derive an expression for the voltage gain in terms of \( g_m \) and the resistances.

Answer

\[
A_v = \frac{-g_m R_L'}{1 + g_m R_S}
\]
5.10 Evaluate the gain expression found in Exercise 5.9 by using the values given in Example 5.6. Compare the result with the voltage gain found in the example.

Answer $A_v = -0.849$ without the bypass capacitor, compared to $A_v = -5.66$ with the bypass capacitor in place. Unbypassed impedance between the FET source terminal and ground greatly reduces the gain of a common-source amplifier.

5.6 THE SOURCE FOLLOWER

Another amplifier circuit, known as a source follower, is shown in Figure 5.33. The signal to be amplified is $v(t)$, and $R$ is the internal resistance of the signal source. The coupling capacitor $C_1$ causes the ac input signal to appear at the gate of the FET. The capacitor $C_2$ connects the load to the source terminal of the MOSFET. (In the midband analysis of the amplifier, we assume that the coupling capacitors behave as short circuits.) The resistors $R_S$, $R_1$, and $R_2$ form the bias circuit.

The Small-Signal Equivalent Circuit

The small-signal equivalent circuit is shown in Figure 5.34. The coupling capacitors have been replaced by short circuits, and the FET has been replaced by its small-signal equivalent. Notice that the drain terminal is connected directly to ground, because the dc supply becomes a short in the small-signal equivalent. Here, the FET equivalent circuit is drawn in a different configuration (i.e., with the drain at the bottom) from that illustrated earlier, but it is the same electrically.

![Figure 5.33 Source follower.](image)
Figure 5.34 Small-signal ac equivalent circuit for the source follower.

Drawing the small-signal equivalent of an amplifier circuit is an important skill for electronics engineers. Starting from Figure 5.33, test yourself to see if you can obtain the small-signal circuit.

**Voltage Gain**

We now derive an expression for the voltage gain of the source follower. Notice that \( r_d \), \( R_S \), and \( R_L \) are in parallel. We denote the parallel combination by

\[
R'_L = \frac{1}{1/r_d + 1/R_S + 1/R_L} \tag{5.44}
\]

The output voltage is given by

\[
v_o = \beta_m v_{gs} R'_L \tag{5.45}
\]

Furthermore, we can write the following voltage equation:

\[
v_{in} = v_{gs} + v_o \tag{5.46}
\]

Using Equation (5.45) to substitute for \( v_o \) in Equation (5.46), we have

\[
v_{in} = v_{gs} + \beta_m v_{gs} R'_L \tag{5.47}
\]

Dividing the respective sides of Equations (5.45) and (5.47), we obtain the following expression for the voltage gain:

\[
A_v = \frac{v_o}{v_{in}} = \frac{\beta_m R'_L}{1 + \beta_m R'_L} \tag{5.48}
\]

Notice that the voltage gain given in Equation (5.48) is positive and less than unity. Thus, the source follower is a noninverting amplifier with voltage gain slightly less than unity.

**Input Resistance**

The input resistance is the resistance seen looking into the input terminals of the equivalent circuit. Hence, we have

\[
R_{in} = \frac{v_{in}}{i_{in}} = R_G \tag{5.49}
\]
Figure 5.35 Equivalent circuit used to find the output resistance of the source follower.

**Output Resistance**

To find the output resistance, we remove the load resistance, replace the signal source with its internal resistance, and look back into the output terminals. It is helpful to attach a test source $v_x$ to the output terminals as illustrated in Figure 5.35. Then the output resistance is

$$R_o = \frac{v_x}{i_x}$$  \hspace{1cm} (5.50)

where $i_x$ is the current supplied by the test source as shown in the figure. The output resistance is given by

$$R_o = \frac{1}{g_m + 1/R_S + 1/r_d}$$  \hspace{1cm} (5.51)

This resistance can be quite low, and another reason for using a source follower is to obtain low output resistance.

**Example 5.8  Gain and Impedance Calculations for a Source Follower**

Consider the source follower illustrated in Figure 5.33, given that $R_L = 1\ \text{k}\Omega$ and $R_1 = R_2 = 2\ \text{M}\Omega$. The NMOS transistor has $K_P = 50\ \mu\text{A}/\text{V}^2$, $\lambda = 0$, $L = 2\ \mu\text{m}$, $W = 160\ \mu\text{m}$, and $V_{th} = 1\ \text{V}$. Find the value required for $R_S$ to achieve $I_DQ = 10\ \text{mA}$. Then compute the voltage gain, input resistance, and output resistance.

**SOLUTION** From Equations (5.3) and (5.5), we have

$$K = \left(\frac{W}{L}\right)\frac{K_P}{2} = 2\ \text{mA}/\text{V}^2$$

and

$$I_{DQ} = K(V_{GSDQ} - V_{th})^2$$

Solving the latter equation for $V_{GSDQ}$ and substituting values, we obtain

$$V_{GSDQ} = \sqrt{I_{DQ}/K} + V_{th} = 3.236\ \text{V}$$
The dc voltage at the gate terminal is given by
\[ V_G = V_{DD} \times \frac{R_2}{R_1 + R_2} = 7.5 \text{ V} \]

The dc voltage at the source terminal of the NMOS is
\[ V_S = V_G - V_{GSQ} = 4.264 \text{ V} \]

Finally, we find the source resistance:
\[ R_S = \frac{V_S}{I_{DQ}} = 426.4 \text{ } \Omega \]

(Of course, in a discrete circuit, we would choose a standard nominal value for \( R_S \). However, we will continue this example using the exact value computed for \( R_S \).)

Next, we use Equation (5.30) to find the transconductance of the device:
\[ g_m = \sqrt{2KP} \sqrt{W/L} \sqrt{I_{DQ}} = 8.944 \text{ mS} \]

Because we have \( \lambda = 0 \), the drain characteristics are horizontal in the saturation region, and \( r_d = \infty \).

Next, we substitute values into Equation (5.44):
\[ R'_L = \frac{1}{1/r_d + 1/R_S + 1/R_L} = 298.9 \text{ } \Omega \]

Then the voltage gain is given by Equation (5.48):
\[ A_v = \frac{v_o}{v_{in}} = \frac{g_m R'_L}{1 + g_m R_L} = 0.7272 \]

The input resistance is
\[ R_n = R'_L = 1 \text{ M}\Omega \]

The output resistance is given by Equation (5.51):
\[ R_o = \frac{1}{g_m + 1/R_S + 1/r_d} = 88.58 \text{ } \Omega \]

This is a fairly low output resistance compared with that of other single-FET amplifier configurations.

The current gain can be found by the use of Equation (1.4):
\[ A_i = A_v \frac{R_{in}}{R_L} = 727.2 \]

The power gain is given by
\[ G = A_v A_i = 528.8 \]

Even though the voltage gain is less than unity, the output power is much greater than the input power because of the high input resistance.

\[ \Box \]
The source follower has voltage gain slightly less than unity, high input impedance, and low output impedance. The current gain and power gain can be larger than unity.

In the preceding section and in this one, we have considered two of the most important single-stage FET amplifiers: the common-source amplifier and the source follower. Later in the book, we discuss other amplifier configurations that use FETs, multistage amplifiers, and amplifiers that use both FETs and BJTs.

**EXERCISE**

5.11 Derive Equation (5.51).

**EXERCISE**

5.12 Derive expressions for the voltage gain, input resistance, and output resistance of the common-gate amplifier illustrated in Figure 5.36.

**Answer** The small-signal equivalent circuit is shown in Figure 5.37. $A_v = g_mR'_L$ in which $R'_L = R_D || R_L$; $R_{in} = 1/(g_m + 1/R_S)$; $R_o = R_D$.

![Figure 5.37](image)

See Exercise 5.12.
5.19. What is the largest value of $R_D$ allowed in the circuit of Problem 5.18 if the instantaneous operating point is required to remain in the saturation region at all times?

5.20. The distorted signal shown in Figure 5.15 can be written as

$$v_{DS}(t) = V_{DC} + V_{in} \sin(2000\pi t) + V_{in} \cos(4000\pi t)$$

The term $V_{in} \sin(2000\pi t)$ is the desired signal. The term $V_{in} \cos(4000\pi t)$ is distortion, which in this case has twice the frequency of the input signal and is called second-harmonic distortion. Determine the values of $V_{in}$ and $V_{in}$ and the percentage of second-harmonic distortion, which is defined as $|V_{in} / V_{in}| \times 100\%$. (A high-quality audio amplifier has a distortion percentage less than 0.1%).

Section 5.3: Bias Circuits

5.21. The fixed- plus self-bias circuit of Figure 5.16 has $V_{DD} = 15\, V$, $R_1 = 2\, M\Omega$, $R_2 = 1\, M\Omega$, $R_3 = 4.7\, k\Omega$, and $R_D = 4.7\, k\Omega$. The MOSFET has $V_{th} = 1\, V$, $\lambda = 0$, and $K = 0.25\, mA/V^2$. Determine the Q-point.

5.22. Find $I_{DS}$ and $V_{DSQ}$ for the circuit shown in Figure 5.22. The MOSFET has $V_{th} = 1\, V$, $\lambda = 0$, and $K = 0.25\, mA/V^2$. Find $I_{DS}$ and $V_{DSQ}$ for the circuit shown in Figure 5.22. The MOSFET has $V_{th} = 1\, V$, $\lambda = 0$, and $K = 0.25\, mA/V^2$.

5.23. (a) Find the value of $I_{DS}$ for the circuit shown in Figure 5.23. Assume that $V_{th} = 4\, V$, $\lambda = 0$, and $K = 1\, mA/V^2$. (b) Repeat for $V_{th} = 2\, V$, $\lambda = 0$, and $K = 2\, mA/V^2$.

5.24. Fixed- plus self-bias circuit design. Design a fixed- plus self-bias circuit for a common-source NMOS amplifier. Nominally, the transistor has $KP = 50\, \mu A/V^2$, $W = 80\, \mu m$, $L = 10\, \mu m$, $\lambda = 0$, and $V_{th} = 1\, V$. The circuit is to have $V_{DD} = 12\, V$ and $I_{DS} \equiv 1\, mA$. We suggest these design guidelines for the NMOS bias circuit for the common-source amplifier: $R_D I_{DS} = V_{DD}/2$; $V_{DSQ} = V_{DD}/2$; $R_S I_{DS} = V_{DD}/4$.

5.25. Fixed- plus self-bias circuit design. Design a fixed- plus self-bias circuit for an NMOS source follower. Nominally, the transistor has $KP = 50\, \mu A/V^2$, $W = 80\, \mu m$, $L = 10\, \mu m$, $\lambda = 0$, and $V_{th} = 1\, V$. The circuit is to have $V_{DD} = 12\, V$ and $I_{DS} \equiv 1\, mA$. We suggest these design guidelines for the NMOS bias circuit for the source follower: $V_{DSQ} \equiv V_{DD}/2$ and $R_S I_{DS} = V_{DD}/4$.

5.26. Find $I_{DS}$ and $V_{DSQ}$ for the circuit shown in Figure 5.26. The MOSFET has $V_{th} = 1\, V$, $\lambda = 0$, and $K = 0.25\, mA/V^2$.

5.27. Find $I_{DS}$ and $V_{DSQ}$ for the circuit displayed in Figure 5.27. The MOSFET has $V_{th} = 1\, V$, $\lambda = 0$, and $K = 0.25\, mA/V^2$. 

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Figure P5.18

Figure P5.23

Figure P5.22

Figure P5.26
5.28. Draw the small-signal equivalent circuit for a FET, including $r_d$.

5.29. Give definitions of $g_m$ and $r_d$ as partial derivatives.

5.30. A certain NMOS transistor has $\lambda = 0$. What is the value of $r_d$, assuming operation in the saturation region?

5.31. What is the value of $g_m$ for $V_{DSQ} = 0$? Draw the small-signal equivalent circuit at this bias point. For what applications is the FET used at this bias point?

5.32. Derive an expression for $g_m$ in terms of $K$, $V_t$, $V_{GSQ}$, and $I_{DQ}$ for an NMOS transistor operating in the triode region. Assume that $\lambda = 0$.

5.33. Derive an expression for $r_d$ in terms of $K$, $V_t$, $V_{GSQ}$, and $V_{DSQ}$ for an NMOS transistor operating in the triode region. Assume that $\lambda = 0$.

5.34. A certain NMOS transistor has $K_P = 50 \mu A/V^2$, $\lambda = 0.1$, $L = 2 \mu m$, $W = 100 \mu m$, and $V_t = 1 V$.

(a) Use a SPICE program to produce a plot of the drain characteristics of this transistor for $V_{DS}$ ranging from 0 to 10 V and $V_{GS}$ ranging from 1 to 3 V.

(b) Use the characteristics plotted in part (a) to graphically determine the values of $g_m$ and $r_d$ at the operating point defined by $V_{DSQ} = 8 V$ and $V_{GSQ} = 2 V$.

(c) Devise a circuit for this transistor so that it operates at the $Q$-point defined in part (b). Use SPICE to perform an operating-point analysis of your circuit. Then find the values of $g_m$ and $r_d$ in the output file, and compare them with the values found in part b. (P Spice refers to $1/r_d$ as GDS.)

5.35. A certain NMOS transistor has $K_P = 50 \mu A/V^2$, $\lambda = 0.1$, $L = 2 \mu m$, $W = 100 \mu m$, and $V_t = 1 V$. Use SPICE to obtain a plot of $g_m$ versus $I_{DQ}$ for $V_{DSQ} = 8 V$. Allow $V_{DSQ}$ to range from 0 to 3 V. (Hint: Simulate the circuit shown in Figure 5.7 with $V_{DS} = 8 V$. Sweep $V_{GS}$ from 0 to 3 V. Then use Probe to obtain a plot of $dI_D/dV_{GS}$ versus $I_D$.)

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**Section 5.5: The Common-Source Amplifier**

5.36. What is the function of coupling capacitors? With what are they replaced in a midband small-signal equivalent circuit? In general, what effect do coupling capacitors have on the gain of an amplifier as a function of frequency?


5.38. Consider the amplifier illustrated in Figure P5.38.

(a) Draw the small-signal midband equivalent circuit.

(b) Assume that $r_d = \infty$, and derive expressions for the voltage gain, input resistance, and output resistance.

(c) Find $I_{DQ}$ if $R = 100 k\Omega$, $R_f = 100 k\Omega$, $R_D = 3 k\Omega$, $R_L = 10 k\Omega$, $V_{DD} = 20 V$, $V_{DD} = 5 V$, and $K = 1 m\AA/V^2$. Determine the value of $g_m$ at the $Q$-point.

(d) Evaluate the expressions found in part (b).

(e) Find $v_o(t)$ if $v(t) = 0.2 \sin(2000\pi t)$.

(f) Is this amplifier inverting or noninverting? Would you classify the input resistance as high, moderate, or low compared with that of other types of FET amplifier?
\[ K = \frac{W}{L} \frac{KP}{2} \quad KP = \frac{\mu}{n} C_{ox} \]

For \( v_{in} = +1 \) we have \( v_{GS} = 4 \) and the instantaneous operating point is A. Similarly for \( v_{in} = -1 \) we have \( v_{GS} = 2 \) V and the instantaneous operating point is at B. We find \( V_{DSQ} \approx 11 \) V, \( V_{DSmin} \approx 6 \) V, \( V_{DSmax} \approx 14 \) V.

**Exercise 5.4**

The analysis is similar to Example 5.3 in the book.

\[ K = \left( \frac{W}{L} \right) \frac{KP}{2} = 1 \text{ mA/V}^2 \]
\[ V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 20 \frac{1}{(1.5 + 1)} = 8 \text{ V} \]

\[ V_{GSQ}^2 + \left( \frac{1}{R_{SK}} - 2V_{to} \right)V_{GSQ} + (V_{to})^2 - \frac{V_G}{R_{SK}} = 0 \]

After values are substituted, we have

\[ V_{GSQ}^2 - 3.583V_{GSQ} + 0.6667 = 0 \]

Solving we find \( V_{GSQ} = 3.39 \text{ V} \). (The second root is extraneous and should be discarded.) Then we have

\[ I_{DQ} = K(V_{GSQ} - V_{to})^2 = 1.92 \text{ mA} \]

\[ V_{DSQ} = V_{DD} - (R_D + R_S)I_{DQ} = 10.8 \text{ V} \]

**Exercise 5.5**

We should choose \( R_D = 0 \) for a source follower. Many values will work for the other resistors. A reasonable set of values is \( R_S = 3.9 \text{ k} \Omega \), \( R_1 = 1 \text{ M} \Omega \), and \( R_2 = 2 \text{ M} \Omega \). These values yield \( I_{DQ} = 1.98 \text{ mA \ and \ } V_{DSQ} = 7.26 \text{ V} \). Use SPICE to check that your design provides a Q-point close to the desired value.

**Exercise 5.6**

From Figure 5.24 at an operating point defined by \( V_{GSQ} = 2.5 \text{ V} \) and \( V_{DSQ} = 6 \text{ V} \), we have

\[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(4.4 - 1.1) \text{ mA}}{1 \text{ V}} = 3.3 \text{ mS} \]

\[ 1/R_d = \frac{\Delta I_D}{\Delta V_{DS}} = \frac{(2.9 - 2.3) \text{ mA}}{14 - 2 \text{ V}} = 0.05 \times 10^{-3} \]

Taking the reciprocal, we find \( r_d = 20 \text{ k} \Omega \)

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\[ 11 = V_{DC} + V_{2m} \]

and at \( t = 0.75 \text{ ms} \) we have:

\[ 16 = V_{DC} - V_{1m} - V_{2m} \]

Solving the previous three equations we have \( V_{DC} = 10.5 \text{ V}, \) \( V_{2m} = 0.5 \text{ V} \) and \( V_{1m} = -6 \text{ V} \). Thus the percentage second-harmonic distortion is \( |V_{2m}/V_{1m}| \times 100\% = 8.33\% \).

**Problem 5.21**

First, we use Equation 5.16 to compute

\[ V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 5 \text{ V} \]

As in Example 5.3, we need to solve:

\[ V_{GSQ}^2 + \left[ \frac{1}{R_{SK}} - 2V_{to} \right] V_{GSQ} + (V_{to})^2 - \frac{V_G}{R_{SK}} = 0 \]

Substituting values, we have

\[ V_{GSQ}^2 - 1.1489V_{GSQ} - 3.2553 = 0 \]

The roots are \( V_{GSQ} = 2.4679 \text{ V} \) and \(-1.319 \text{ V} \). The correct root is \( V_{GSQ} = 2.4679 \text{ V} \) which yields \( I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.5387 \text{ mA} \). Finally we have \( V_{DSQ} = V_{DD} - R_{D^1} I_{DQ} - R_S I_{DQ} = 9.936 \text{ V} \).

**Problem 5.22**

For this circuit we can write

\[ V_{GSQ} = 15 - I_{DQ} R_S \]

Assuming operation in saturation, we have

\[ I_{DQ} = K(V_{GSQ} - V_{to})^2 \]

using the first equation to substitute into the second equation we have

\[ I_{DQ} = K(15 - I_{DQ} R_S - V_{to})^2 = 0.25(14 - 3I_{DQ})^2 \]
where we have assumed that $I_{DQ}$ is in mA. Rearranging we have

$$I_{DQ}^2 - 9.777I_{DQ} + 21.777 = 0$$

The correct root is the smaller one which is $I_{DQ} = 3.432$ mA. Then we have $V_{DSQ} = 30 - R_D I_{DQ} - R_S I_{DQ} = 16.27$ V.

**Problem 5.23**

Assuming that the MOSFET is in saturation, we have

$$V_{GSQ} = 10 - I_{DQ}$$

$$I_{DQ} = K(V_{GSQ} - V_t)^2$$

where we have assumed that $I_{DQ}$ and $K$ are in mA and mA/V$^2$ respectively.

(a) Using the second equation to substitute in the first, substituting values and rearranging, we have

$$V_{GSQ}^2 - 7V_{GSQ} + 6 = 0$$

which yields

$$V_{GSQ} = 6 \text{ V}$$

(The other root, $V_{GSQ} = 1$ V, is extraneous.)

$$I_{DQ} = 4 \text{ mA}$$

$$V_{DSQ} = 10 - 2I_{DQ} = 12 \text{ V}$$

(b) Similarly we have

$$V_{GSQ}^2 - 3.5V_{GSQ} - 1 = 0$$

$$V_{GSQ} = 3.765 \text{ V}$$

$$I_{DQ} = 6.234 \text{ mA}$$

$$V_{DSQ} = 20 - 2I_{DQ} = 7.53$$

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Problem 5.26

We have \( V_G = V_{GSQ} = \frac{10R_2}{(R_1 + R_2)} = 2.5 \text{ V} \). Then we have
\[
I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.5625 \text{ mA}, \quad V_{DSQ} = V_{DD} - R_D I_{DQ} = 4.375 \text{ V}.
\]

Problem 5.27

We have \( V_{GSQ} = V_{DSQ} = V_{DD} - R_D I_{DQ} \). Then substituting \( I_{DQ} = K(V_{GSQ} - V_{to})^2 \), we have
\[
V_{GSQ} = V_{DD} - R_D K(V_{GSQ} - V_{to})^2
\]
Substituting values and rearranging, we have
\[
V_{GSQ}^2 + 2V_{GSQ} - 39 = 0
\]
Solving we determine that \( V_{GSQ} = 5.325 \text{ V} \) and then we have \( I_{DQ} = K(V_{GSQ} - V_{to})^2 = 4.675 \text{ mA} \).

Problem 5.28

See Figure 5.23 in the book.

Problem 5.29

\[
g_m = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_{Q-point} \quad \frac{1}{r_d} = \left. \frac{\partial i_D}{\partial V_{DS}} \right|_{Q-point}
\]

Problem 5.30

For \( \lambda = 0 \) the drain characteristics are horizontal in the saturation region and \( r_d = \infty \).
Problem 5.37

See Figure 5.25 in the book.

Problem 5.38

(a)

(b) \[ v_o = R'_L (i_{in} - g_m v_{in}) \]
\[ i_{in} = (v_{in} - v_o)/R_f \]

\[ A_v = \frac{v_o}{v_{in}} = \frac{R'_L - g_m R'_f}{R'_L + R_f} \]

\[ R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_f}{1 - A_v} \]

The circuit used to determine output impedance is:

We define \( R'_D = R'D/(R + R_f) \)

\[ v_{gs} = v_x \frac{R}{R + R'_f} \]
\[ i_x = \frac{v_x}{R'_D} + g_m v_{gs} \]
\[ R_o = \frac{V_x}{I_x} = \frac{1}{\frac{1}{R'_D} + \frac{g_m R}{R_f + R}} \]

(c) The dc circuit is:

\[ +V_{DD} = 20 \]

\[ R_f \quad R_D = 3k\Omega \]

\[ V_{GSQ} = V_{DSQ} \quad I_{DQ} = K(V_{DSQ} - V_{to})^2 \quad I_{DQ} = (V_{DD} - V_{DSQ})/R_D \]

Using the above equations we obtain

\[ 3V_{DSQ}^2 - 29V_{DSQ} + 55 = 0 \]

\[ V_{DSQ} = 7.08 \, V \text{ and } I_{DQ} = 4.31 \, mA \]

\[ g_m = g_m = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_{Q-point} = 2K(V_{GSQ} - V_{to}) = 4.16 \times 10^{-3} \, S \]

(d) \[ R'_L = R_D | R_L = 2.31 \, k\Omega \]

\[ A_v = \frac{-9.37}{9.64 \, k\Omega} \]

\[ R_{in} = 414 \, \Omega \]

(e) \[ v_o(t) = v(t) \frac{R_{in}}{R + R_{in}} A_v = -0.164 \sin(2000\pi t) \]

(f) This is an inverting amplifier that has a very low input impedance compared to many other FET amplifiers.

**Problem 5.39**

Referring to the circuit shown in Figure P5.39, we have

\[ V_{GSQ} = V_{DSQ} \quad I_{DQ} = K(V_{GSQ} - V_{to})^2 \quad I_{DQ} = (V_{DD} - V_{DSQ})/R_D \]